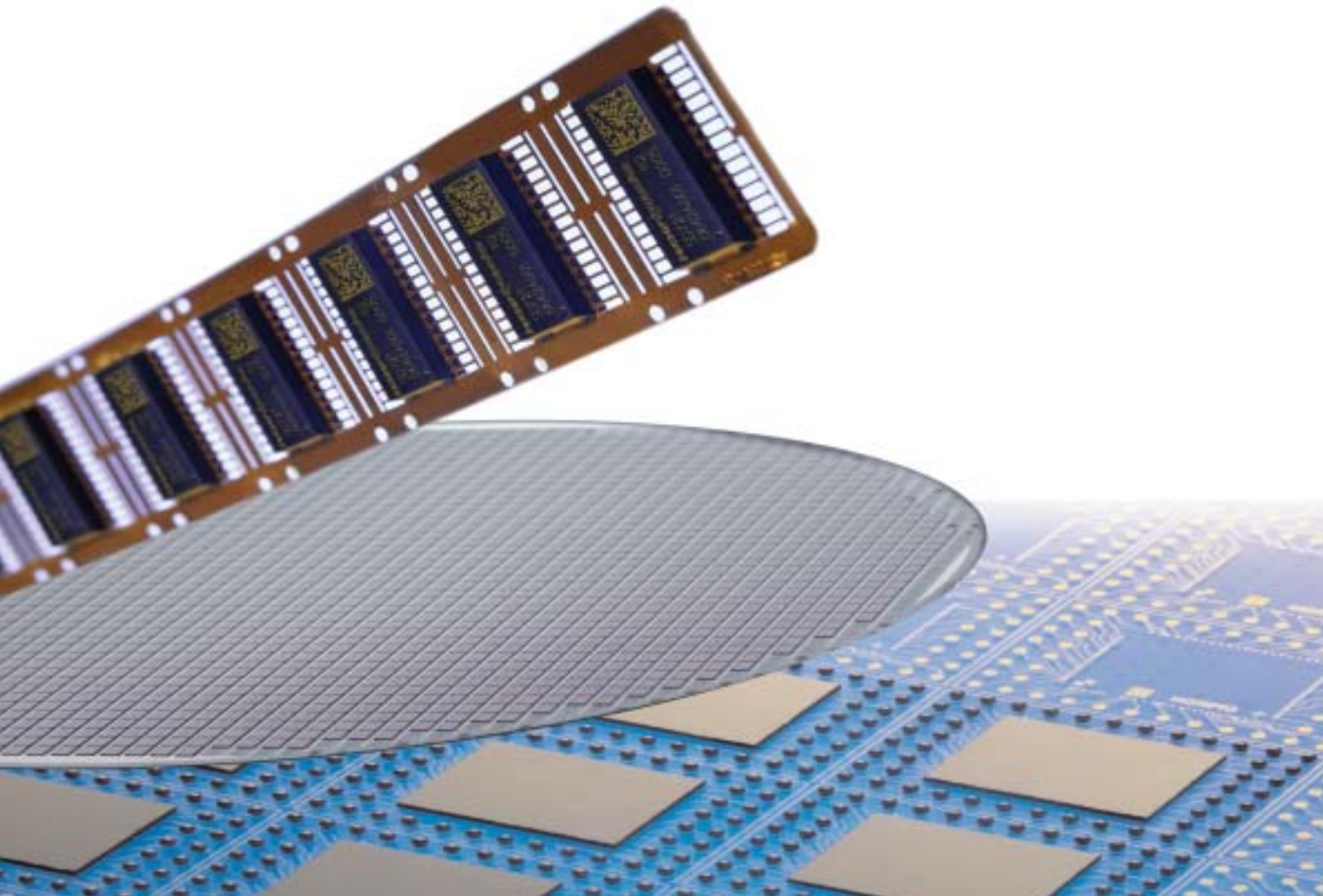
ISIT

Fraunhofer Institut Siliziumtechnologie

Achievements and Results
Annual Report 2007



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Ion implantation in the PowerMOS production cleanroom.

Preface

Dear business partners,
dear friends of the ISIT, dear colleagues,

The year 2007 was another very eventful one for our institute. It was marked by a major change-over of staff and by in-depth research activities in all central areas addressed by ISIT. We experienced what was probably the most pleasing growth in terms of new, trend-setting research projects last year in the field of power electronics. This result testifies to the present-day technological trend in our society.

Power electronics is steadily becoming more important in the context of the increasingly vehement energy debate in Germany, especially when one considers that 40 percent of the overall energy demand is met by electrical energy. One of the main tasks of power electronics in the future is to make more efficient use of this energy, and one way in which we can help to improve energy efficiency is to develop semiconductor elements with lower power dissipation.

On the initiative of ISIT a regional network for power electronics has been set up in Schleswig-Holstein. Funding for the pilot project on power electronics, which is worth 6 million euros, is being supplied in three equal shares by the Land of Schleswig-Holstein, the Fraunhofer-Gesellschaft and several industrial enterprises based in Schleswig-Holstein. These companies are ESW (Jenoptik), Danfoss, Jungheinrich and Vishay, which are primarily contributing their systems know-how and specifications for the high-power electronic circuits of the future. Other research establishments besides the Fraunhofer ISIT are collaborating on this project: the Fachhochschule Westküste in Heide, Fachhochschule in Kiel and the Christian-Albrechts-Universität (CAU) in Kiel.

As the first concrete application, new converter concepts are being drawn up in a pilot project. Converters are the core element of high-power electronic systems which, when used in controlling motors, pumps etc., can result in energy savings of up to 30%. The goal of the network is to develop innovative products for power electronics over and above the pilot project in order to boost competitiveness and create new jobs over the medium term.

The network that now exists is open to further members. Other industries in Schleswig-Holstein to which power electronics is particularly important, such as companies working in the area of renewable power sources, can join the network during the three-year project phase.

I would like to thank the government of Schleswig-Holstein and especially Economics Minister Dietrich Austermann and his staff for helping this project to come about. I am also grateful to Dr. Wöhl, Dr. Feldhütter and Professor Buller of the Fraunhofer-Gesellschaft headquarters, who gave the ISIT their support in initiating this network. Through the network, the institute will be able to acquire many more projects from industry and from the public sector in areas that go far beyond the scope of the pilot topic.

Furthermore, ISIT has initiated a cooperation between the Fraunhofer Institutes working in the power electronics sector (Fraunhofer IZM, Fraunhofer IISB, Fraunhofer ISE, Fraunhofer IAF). These institutes complement one another in the range of services that they offer, thereby covering a large part of the value chain. It comprises devices, packaging technology, reliability analysis and finally system integration. The foremost goal of this cooperation is an inhouse Fraunhofer project to increase energy efficiency, but it is aspired that in the medium term, the collaboration will result in further industrial projects.

It is not only in the power electronics sector that opened up new horizons for the Fraunhofer ISIT in 2007; the institute has also been successful in other areas of its work. It was able to press ahead with one of its most important projects in microsystems engineering, for example. In collaboration with SensorDynamics, ISIT is pursuing the development of high-precision miniaturized angular rate sensors for the automotive industry. One important application of such a sensor is to stabilize the vehicle in bends. ISIT develops these miniaturized elements, which are integrated in a package with a complex electronic evaluation circuit to form

Preface

Markus Richter (middle), Microtechnologist and Bianca Piening (right), Office Clerk, earn the distinction of being the year's best apprentice in the final examination, for which they were awarded a prize by Fraunhofer board member Dr. Dirk-Meints Polter. Left and in the backround: ISIT training officers Jan Lähn and Birgit Gotthard.

ISIT presentation at the Fraunhofer Symposium "Innovation Inside" in Berlin.

More than 2000 guests visited the ISIT presentation at DESY within the framework of the "Nacht des Wissens" in Hamburg. One great attraction was the ISIT photo contest "Mrs. and Mr. Cleanroom".

Electrical biochip packaged in polymeric chipsticks: the heart of automated measuring systems to detect biological agents.

a complete system. In addition to processing the measuring signal, the electronics developed by SensorDynamics undertakes tasks such as self-testing and early identification of malfunctions. The ASIC / Sensor system was successfully qualified for use in the automotive industry at the end of 2007. This makes it possible to offer customers a finished, qualified product. Sensor-Dynamics in Itzehoe is currently getting ready for industrial mass production of these systems.

A very positive change took place at ISIT in the field of biosensors. ISIT has for many years possessed outstanding know-how in research, development and manufacture of biochips for a wide range of applications in the area where microsystems engineering overlaps with biotechnology. This can be attributed particularly to Dr. Rainer Hintsche (German Future Prize 2004) and his working group.

In 2007 an important industrial partner, Analytik Jena AG, was persuaded to invest in this department's spin-off company, eBiochip. This partnership opens up numerous opportunities for AJ eBiochip. The new partner has access to the appropriate markets and possesses the financial strength to make investments and hire additional personnel. Though now a part of Analytik Jena, eBiochip will remain at its ISIT location in Itzehoe, its cooperation with the institute now being governed by contract. This gives ISIT a better opportunity to acquire new projects in collaboration with this strong partner.

ISIT's department on integrated energy systems received a noticeable boost as a result of the automotive industry's change of heart regarding vehicles with hybrid propulsion. New propulsion concepts in the automotive industry (e.g. hybrid electric vehicles) using heavy-duty batteries are coming to the fore as a central issue in Lithium battery technology, not least in light of the present debate on reducing CO_2 emissions. The development of battery systems with a high output, a large capacity and the corresponding degree of reliability and safety, based on the technology developed at ISIT, is therefore set to become a very important topic. In this context, ISIT has succeeded in acquiring projects in the automotive industry for the development of batteries suitable for use in cars.

You will find further details of our 2007 results in the chapter entitled "Representative Results of Work" on pages 31 to 57 of this report.
Our success in the areas of power electronics and microsystems engineering rests to a significant extent on the excellent cooperation between the Fraunhofer ISIT and the Vishay company. Vishay has invested about 60 million U.S. dollars in the Itzehoe site over the past three years to upgrade the entire jointly used semi-conductor production line. Formerly capable of processing wafers with a diameter of 150 mm, the facility is prepared for processing 200 mm wafers. The expansion of this ultra-modern production technology has made it necessary for Vishay to introduce comprehensive research and development activities, with the result that Vishay has further intensified the existing close cooperation with ISIT.

Among the most recent projects for which a funding application has been submitted to the BMBF is the „Super PowerMOS" project, which aims to develop high-voltage PowerMOS elements with a very low power dissipation. The signs that the ministry will grant the requested funds are very positive, so that work on this project will probably be able to start in the spring of 2008. ISIT will have to convert its facilities to 200 mm wafers at the same time as Vishay does. To this end, the Fraunhofer headquarters has provided ISIT with funds to procure the 200 mm equipment needed for development of the inertial sensors. The installation of the equipment will be completed in spring of 2008.

However, the current phase of strong growth in power electronics and microsystems engineering and the rapid expansion of the range of applications has brought the institute to the limits of its capacity in terms of space.
All resources in the ISIT cleanroom facilities are being used to full capacity. In order to

continue to operate with the same high standard of quality in its development and research activities connected with the abundant industrial topics that arise in future, ISIT has devised a project plan for building new cleanroom resources at the site and providing the right technical equipment to handle future development topics. A further, fundamental stage of expansion is planned in which a new, modern cleanroom laboratory will be set up and equipped. This is a good time to build new cleanroom facilities, particularly because funds from the European Regional Development Fund (ERDF) can be used for the project. ISIT has already drawn up an expansion plan and submitted it to the Land and the Fraunhofer headquarters. The final decision regarding a new cleanroom is expected before the end of 2008.

The Fraunhofer ISIT was able to strengthen its staff links with the research infrastructure in Schleswig-Holstein during 2007. Dr. Ralf Dudde, head of strategy and planning at ISIT, was awarded an honorary professorship at the University of Applied Sciences Westküste, Heide.

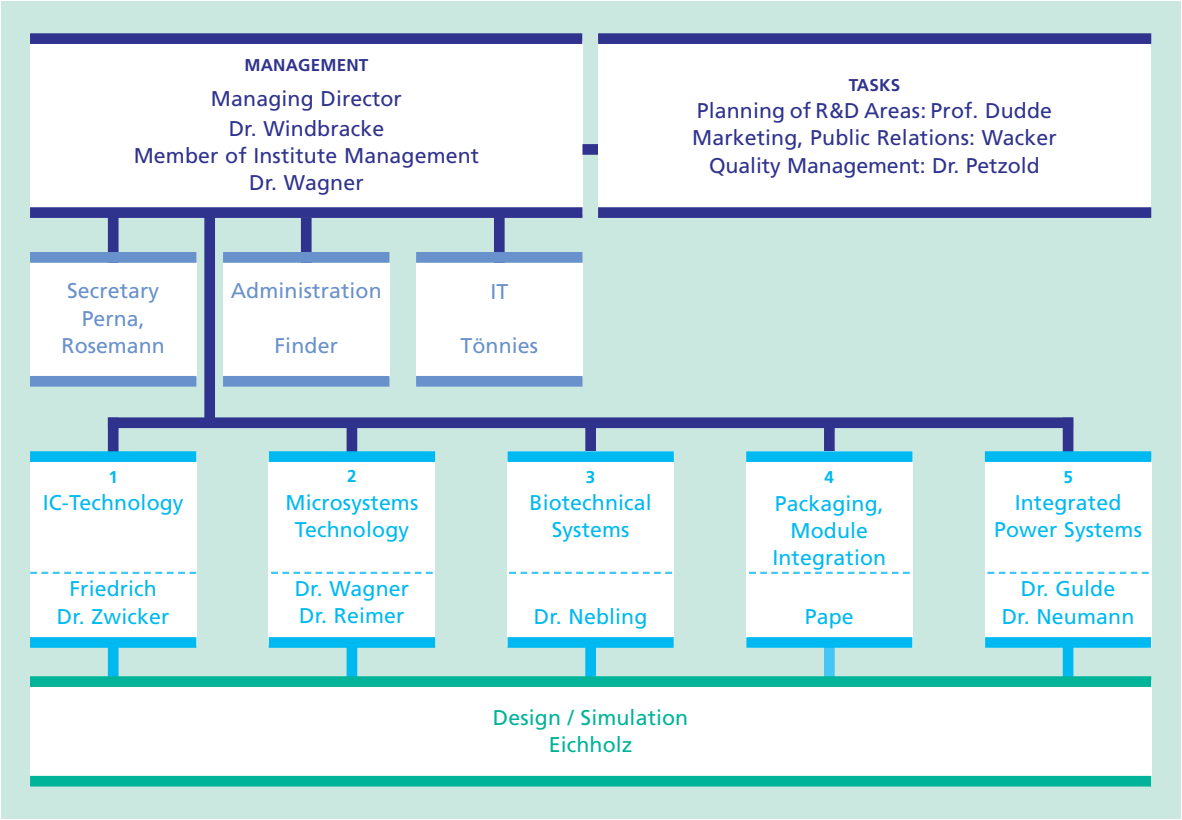
Dr. Bernd Wagner, head of the microsystems engineering department and now deputy director of the institute, was appointed professor at the CAU, institute for materials science, Kiel.

Public distinction for Prof. Anton Heuberger. From left to right: Schleswig-Holstein's premier Peter-Harry Carstensen, Prof. Anton Heuberger and his wife Ingrid, Dr. Wolfgang Windbracke and chief magistrate of Steinburg Hans-Friedrich Tiemann.

These appointments will open up opportunities for collaboration that reach far beyond the initial cooperation in the power electronics network – for example in the field of nanosystems engineering. Taken in conjunction with the new research focus on „Nanosystems Engineering" at Kiel University's Faculty of Engineering (TF), the planned extension of the ISIT now affords an outstanding opportunity to significantly strengthen the connection between the TF and the ISIT and to pool the expertise of the two establishments. The CAU's expertise in materials science and electrical engineering will enable ISIT to supplement and reinforce its preliminary scientific research and thus prepare the basis for the new strategic research areas of the future.

A new generation took over at ISIT in 2007. Some of our most distinguished staff retired from the institute for age reasons, and others will be leaving us during the next few months.
The first person I would like to name is Professor Anton Heuberger, the institute's former director, who retired in March. His name is inseparably linked with the development of the Fraunhofer ISIT and the establishment of Itzehoe as a high-tech center, as well as with the implementation of modern microtechnology in small and medium-sized enterprises, both in Germany and far beyond its borders. It was through his untiring efforts, which went far beyond his professional obligations, that the institute gained its international reputation as a successful research and technology transfer establishment. The German president decorated him with the cross of merit on ribbon of the Order of Merit of the Federal Republic of Germany for his outstanding services. Schleswig-Holstein's premier, Peter Harry Carstensen, presented him with the award at the state government guesthouse in Kiel on August 14.

Until a successor for Prof. Heuberger has been appointed, I myself have provisionally taken over the directorship of the institute. Professor Heuberger is not the only long-standing researcher to have reached retirement age. Others are Dr. Wilhelm Brünger, an expert in the



ISIT Organigram

field of electron beam lithography, whose research work has done a great deal to enhance the institute's international scientific reputation over the years; Dr. Helmut Bernt, a theorist and mentor at the institute, who kept up the contacts with universities during his time at ISIT and supervised many generations of doctoral candidates; Dr. Eike Krullmann, who played a decisive part in setting up the institute cleanroom, and Dr. Rainer Hintsche, who has received important research prizes such as the Philip Morris Prize and the German Future Prize, the German president's prize for technology and innovation. He will be leaving us in a few months' time. However, the expertise of these experienced colleagues will not be lost to the institute. Some of them will continue to place their experience at the disposal of the institute as advisors on various tasks. As managing director of AJ eBiochip, Dr. Hintsche will remain in close contact with the institute.

Non-academic vocational training at ISIT has undergone a very positive development.
For the third time, following 2005 and 2006, ISIT trainees were once again the best at any Fraunhofer institute in their year, passing their final exams with the grade „very good" or as the best in their professional association. This time Bianca Piening (administrative assistant) and Markus Richter (microtechnologist) each achieved one of the highest final examination results in the Fraunhofer-Gesellschaft. Together with their instructors, they were honored for their outstanding examination results by Dr. Dirk-Meints Polter during a ceremony held at the Fraunhofer headquarters in Munich on November 8, 2007.

All the achievements mentioned are the result of the untiring commitment of the ISIT staff. It is my privilege to express my thanks specifically to all my colleagues for their highly qualified performance and for the dedication that they have displayed.

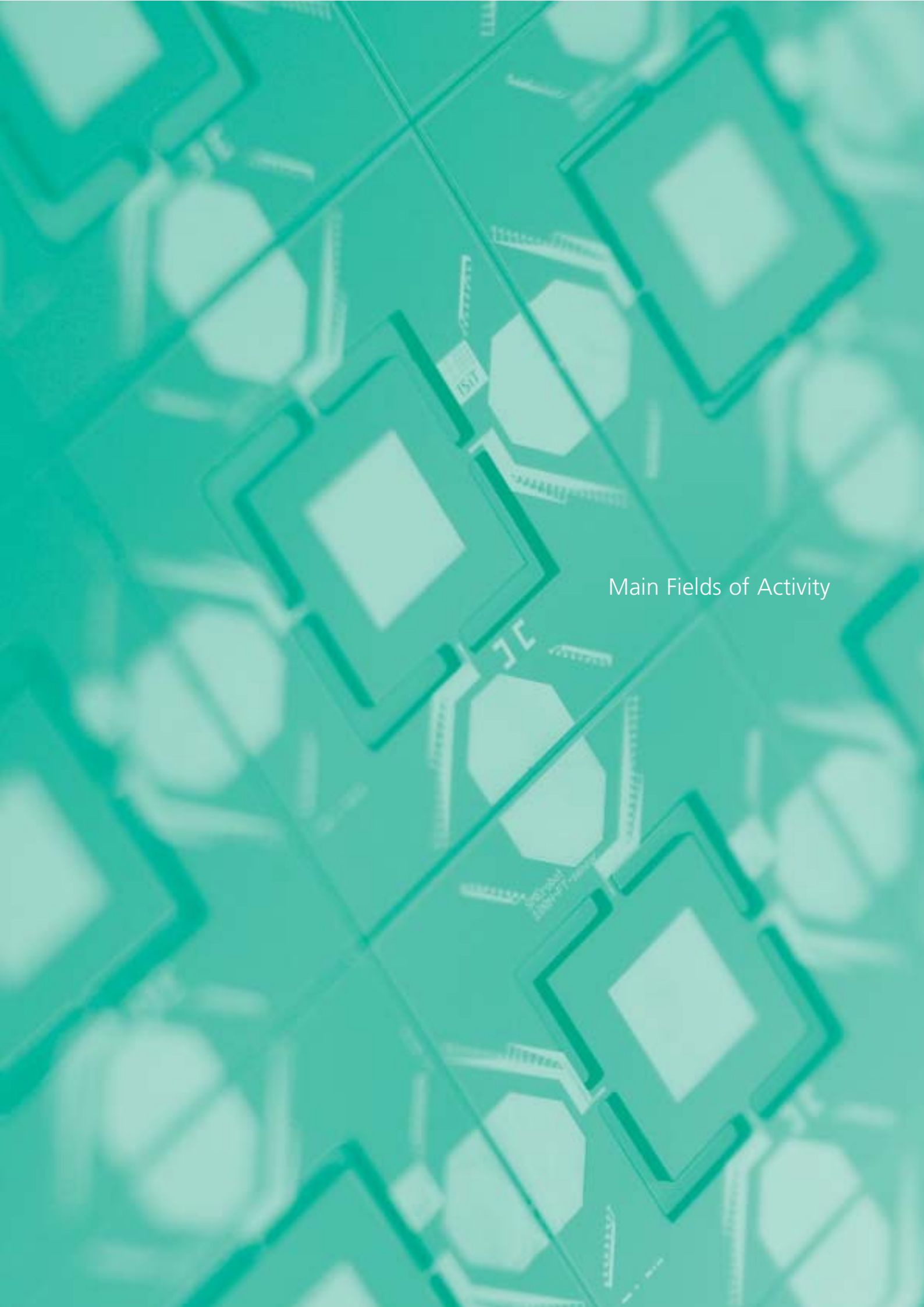
Wolfgang Windbracke

Fraunhofer ISIT
Research and Production at one Location

Fraunhofer ISIT develops and manufactures components in microelectronics and microsystems technology, from the design phase – including system simulation – to prototyping and fabrication of samples, up to series production. Even though components, manufactured at Fraunhofer ISIT such as acceleration sensors, valves, and deflection mirrors often measure just a fraction of a millimeter in size, there is a wide range of applications: the devices are implemented in areas like medical care, environmental and traffic engineering, communication systems, automotive industry, and mechanical engineering. Working under contract, ISIT develops these types of components in accordance with customer requirements, also creating the applications-pecific integrated circuits (ASICs) needed for the operation of sensors and actuators. Included in this service is the system integration using miniaturized assembly and interconnection technology.
Together with Vishay Siliconix Itzehoe GmbH, the institute operates a professional semiconductor production line which is up-to-date in all required quality certifications (e. g. ISO 9001, TS 16949). This line is used in parallel for PowerMOS and microsystem production and for R&D projects developing new devices and technological processes.

Other fields of activity at ISIT focus on assembly and packaging techniques for microsystems, analyze the quality and reliability of electronic components, and develop advanced power-supply components for electronic systems. The institute employs a staff of around 150 people.

Reactive Ion Etching (RIE) tools in the PowerMOS production cleanroom.



Main Fields of Activity

IC Technology and Power Electronics

The power electronics and IC technology group develops and manufactures active integrated circuits as well as discrete passive components. Among the active components the emphasis lies on power devices such as smart power chips, IGBTs, bi-directional components, PowerMOS circuits and diodes. Thereby ISIT primarily uses Vishay's customized, individual production sequences. Additional support for work in this area is provided by a number of tools for simulation, design and testing. ISIT also benefits from years of experience in the design and manufacturing of CMOS circuits. The development of new processes for advanced power device assembly is a further important research topic.

The passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Materials development and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process. ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers customer-specific silicon components processing in small to medium-sized quantities on the basis of a qualified semiconductor process technology.

To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization. This practice provides the institute with specialized expertise in challenges related to etching, deposition, lithography, and planarization methods.

Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems. The intensive work done by ISIT in this area is supported by a corresponding infrastructure. A special emphasis lies in the application of CMP for the manufacturing of MEMS devices and microsystems.

The institute's CMP application lab is equipped with CMP cluster tools, single- and double-sided polishers and post-CMP cleaning equipment for wafers with 100 to 300 mm in diameter. The CMP group at ISIT works in close relationship to Peter Wolters GmbH since many years, as well as

Waferinspection.

Epitaxy cleanroom (above).

Power Device with ultra thin chips (left).

other semiconductor fabrication equipment manufacturers, producers of consumables, CMP users and chip and wafer manufacturers.

The group's work encompasses the following areas:

- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics (SiO_2, TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and microsystems.

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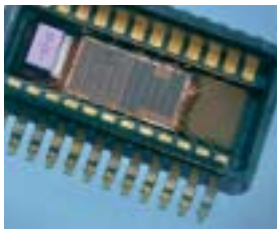
Microsystems Technology (MEMS) and IC Design

Microsystems technology is a core activity at the institute, an area which ISIT has pioneered in Germany. For over 20 years ISIT scientists have been working on the development of micromechanical sensors and actuators, micro-optics, and components for radio-frequency applications (RF-MEMS). Their work in this area also includes integrating these components with microelectronics to create small-size systems of high functionality. A multitude of components and systems have originated at ISIT.



Open cavity package with angular rate sensor and read out ASIC.

Demonstrator of an Inertial Measurement Unit (IMU).

The current emphasis in the area of sensor technology is on inertial sensor technology (acceleration, angular rate, inertial measurement units), pressure, and flow sensors, all with integrated electronics (ASICs). A microsensor core technology using thick polysilicon structural layers and waferlevel hermetic sealing is available.

The development of customized integration concepts, ranging from simple, cost-effective assembly in a common package to complete monolithic integration, represents the core of ISIT's offerings in this area. One integration technique that customers may find particularly valuable is the ability to process microsystems on the surface of a fully processed ASIC wafer using a low-temperature process such as electroplating.

Silicon Wafer with capsulated micro mechanical gyroscopes.

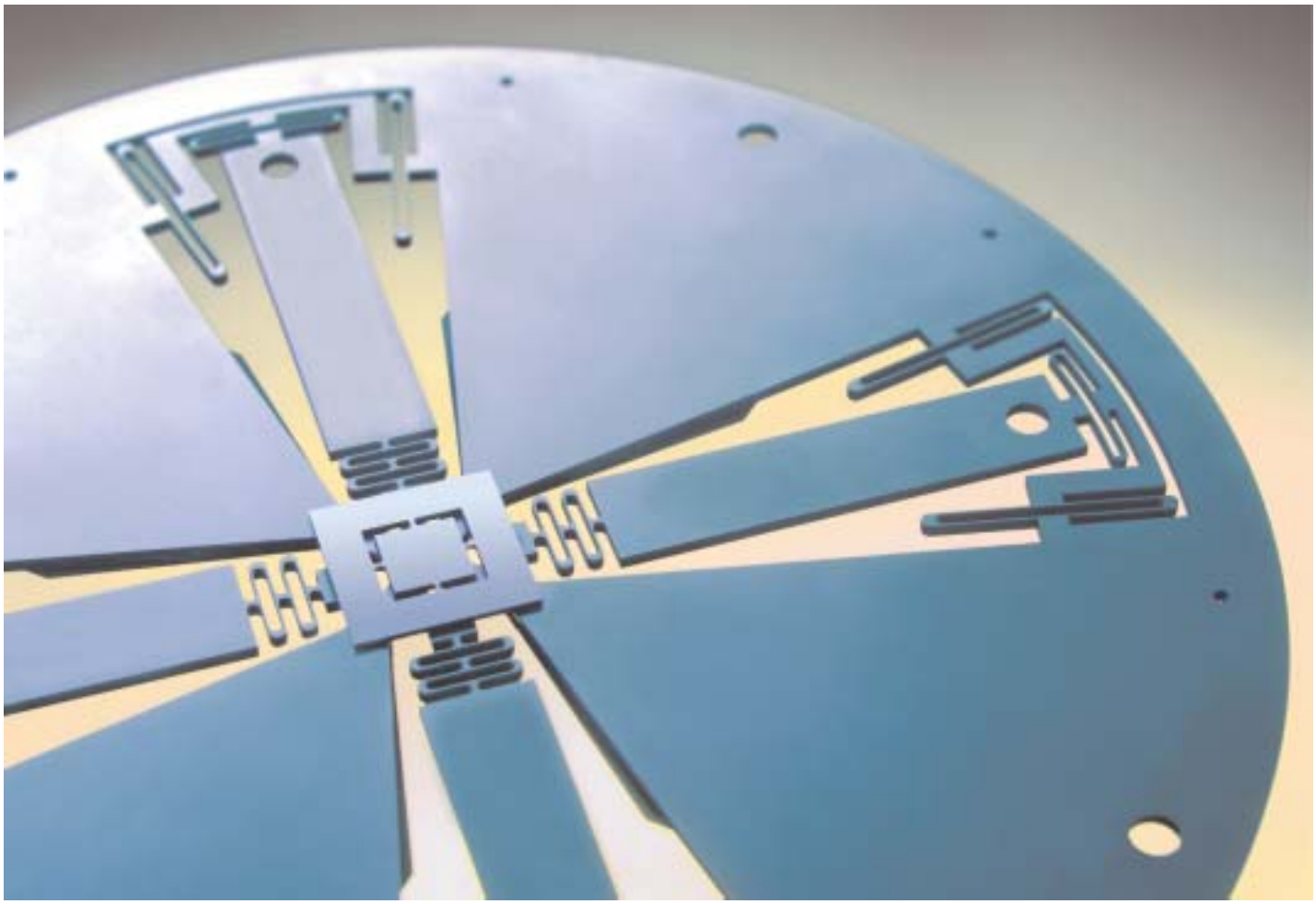
ISIT also develops optical microsystems, primarily for optical instrumentation, consumer products and communication. Examples include micromirrors for laser projection displays, laser scanners and analog or digital light modulators, and passive optical elements such as refractive and diffractive lenses, prisms, or aperture systems.

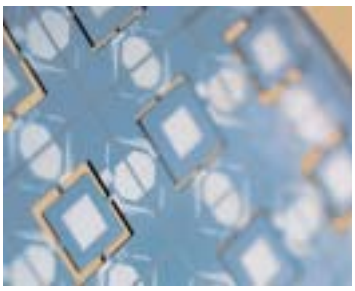
Radio-frequency microsystems developed at ISIT, designed primarily for use in reconfigurable wireless communication devices, include, RF-MEMS switches, tunable capacitors and ohmic switches.

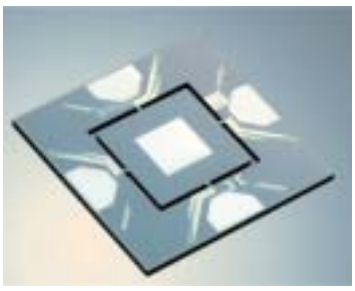
On-chip integrated microactuator systems are especially challenging in order to meet the specific requirements in the micro- and nanometer scale. In this field ISIT has a high expertise and implements electrostatic, thermal and – more recently – high-speed high-force piezoelectric actuation principles on silicon wafers.

The service approach enables ISIT to offer its customers all of these components as prototypes and also to manufacture them in series according to the customer's specific needs, utilizing the quality and capacity of the institute's in-house semiconductor and MEMS production line. The services provided also include application-specific microsystem packaging at wafer level, comprising thin wafer and vertical feedtrough capabilities.

Should a customer's requirements fall outside the scope of the institute's technological capabilities, ISIT can utilize a European network to gain







Force/torque sensors: Sensor in test setup (top);
part of a wafer with sensors (left); single sensor (right).

access to other manufacturers and processes, like production lines at Bosch, SensoNor, HL Planar, ST and Tronic's. ISIT organizes the production as a foundry service for interested customers.

One of the requirements for developing micro-systems and microelectronic components is a highly capable ASIC design group. The staff at ISIT are specialists in the design of analog/digital circuits, which enable the electronic analysis of signals from silicon sensors. The designers at ISIT also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavioral modeling simulation tools.

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Main Fields of Activity

Biotechnical Microsystems

ISIT is a worldwide leader in electrical biochip technology and holds around 20 patents in relevant fields of application. The electrical biochips offer intrinsic advantages over optical biochips because of particle tolerance and mechanical robustness by the direct transduction of biochemical reactions into current measurements. The use of nanometer sized interdigital electrodes, integrated reference and auxiliary electrodes along with ultra-sensitive, ultra-selective measurement techniques (i.e. „redox cycling") enables powerful sensor microarrays. These arrays are useful for the detection of a variety of analytes simultaneously. User-friendly operability is realized by packaging the biochips into cartridges called „Chip-Sticks". In combination with micro-fluidic components and integrated electronics, these electrical microarrays represent the rapid and cost-effective basis of the analysis systems, which can be used to identify and quantify DNA, RNA, proteins and haptens.

ISIT works closely with the Itzehoe based company AJeBiochip GmbH (www.ebiochip.com), an ISIT spin-off, to facilitate the marketing of these new technologies. eBiochip Systems develops a variety of smart and portable instruments, from devices for educational and demonstration purposes to fully automated microarray analysers. The successful application of the platform of electrical biochip technology in a variety of areas including the identification and quantitation of toxic and pathogenic biowarfare agents and the detection of harmful substances in food has been established in several labs in Europe.

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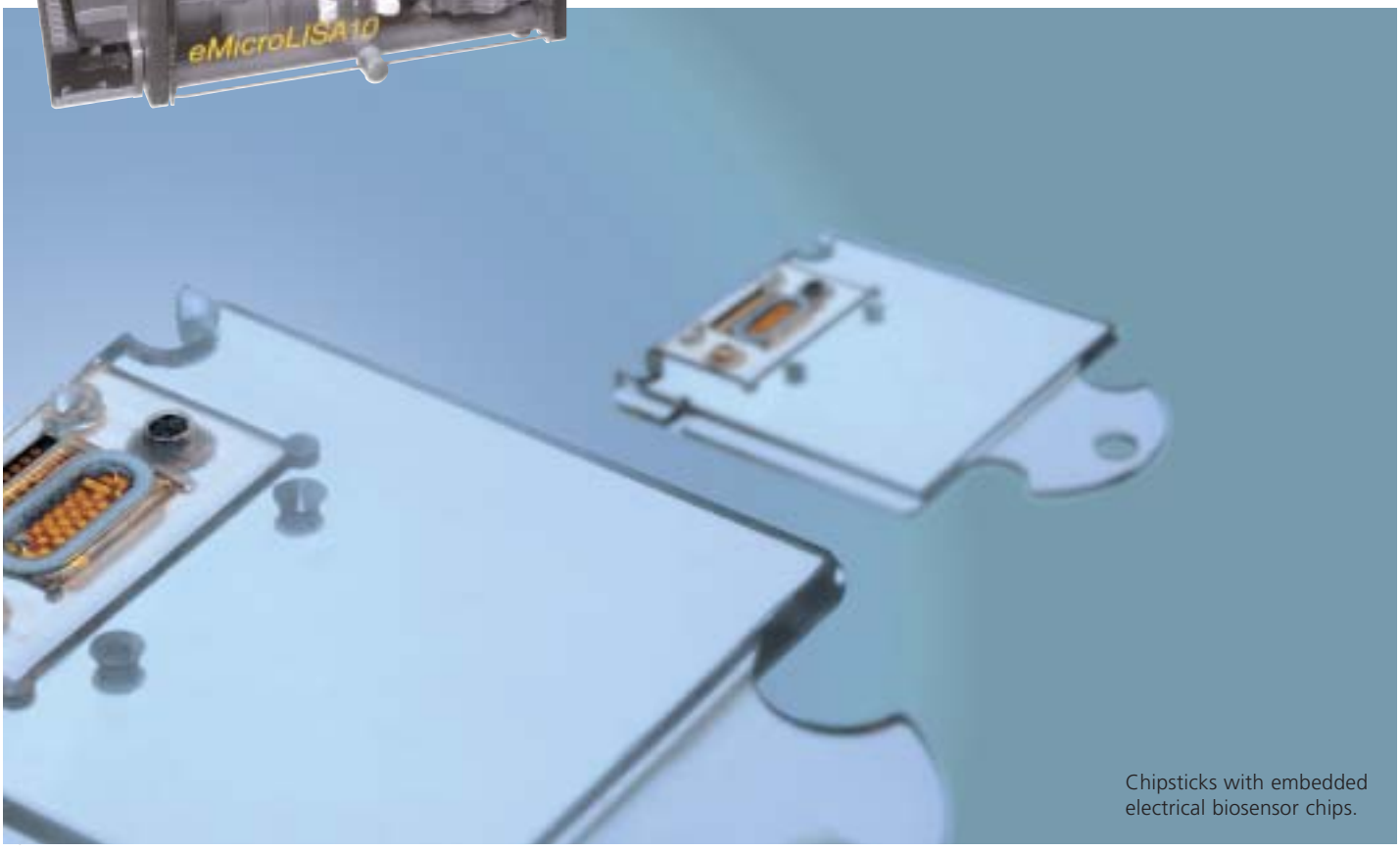
New generation of AJ eBiochip biosensor system with automatical changers for samples and chipsticks.



Chipsticks with embedded electrical biosensor chips.

Packaging Technology for Microelectronics and Microsystems

The assembly and interconnection technology group offers customers a broad range of services, including precision assembly of microstructured components and development and qualification of customer-specific packaging. Work in this area includes hermetic housing and material compatibility tests for assemblies that have to work in aggressive environmental conditions, e.g., development of microsystem packages intended for in vivo use in medical technology.

Another focal area is miniaturization of chip and sensor assemblies and packages, which includes direct assembly of bare silicon chips. The institute possesses capabilities in all of the essential technical stages for chip-on-board (COB) technology, from designing the circuit boards to qualified COB assemblies. The bare ICs and microsensors are mounted using the Chip & Wire or Flip-Chip techniques.

The group also develops processes for assembling, through via generation and packaging chips and sensors/actuators while still on the wafer. Due to the increasing global trend among chip manufacturers to implement this special packaging process, Wafer Level Packaging (WLP) has become a central focus of the group's work.

WLP technology can also be applied for packaging sensors under vacuum, such as angular rate or acceleration sensors. ISIT has successfully integrated thin film getter layers for high-Q microresonators and improved vacuum lifetime.

The institute is active in this area not only as a technology developer, but also as a manufacturer of assemblies for its customers using the available Chip-Size-Packaging pilot production line.

The group also develops ultra-thin electronic assemblies, which involves stacked mounting flexible silicon chips as thin as 50 µm on flexible substrates. These techniques will ultimately lead to further miniaturization in existing systems, such as laptops, hand held PCs or mobile phones, but will also enable the development of new products like intelligent flexible product labels or smart clothes.

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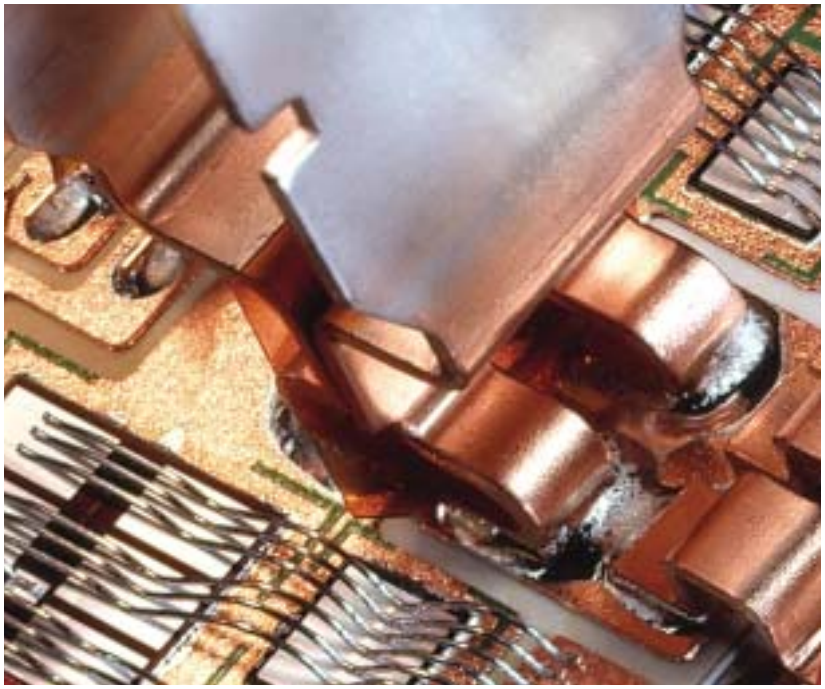
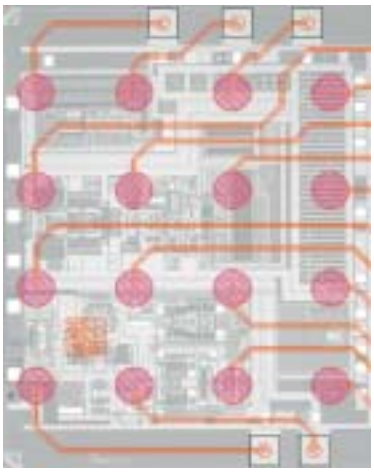


Detail of a power module with 90 µm thin diodes and IGBTs, produced together with Danfoss Silicon Power (right).

Chip-Stacking allows to further increase the functional density of electronic components. Backside contact arrays, e.g. for soldering, are created by through-silicon vias (bottom).



Quality and Reliability of Electronic Assemblies

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, for example whenever new technologies such as lead-free soldering are introduced, when increased error rates are discovered, or if the institute desires to achieve competitive advantages through continual product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as X-ray transmission radiography and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. Then they formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, ISIT is undertaking design, material selection and process modification projects for industrial partners. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company sites.

Online voiding analysis of reflow process by X-ray inspection.

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Demonstration of lead free wave soldering.

Detail: Heating table for reflow process simulation (left).

Integrated Power Systems

Secondary Lithium batteries as a powerful storage medium for electrical energy are rapidly capturing new fields of application outside of the market of portable electronic equipment. Among these new application fields are automotive, medical devices, stationary electric storage units, aerospace, etc. Therefore this type of rechargeable batteries has to meet a variety of new requirements. This covers not only electrical performance but also design and safety features. The Lithium polymer technology developed at ISIT is characterized by an extensive adaptability to specific application profiles like extended temperature range, high power rating, long shelf and/or cycle life, extended safety requirements, etc. Also included is the development of application adapted housings.

In the Lithium polymer technology all components of the cell from electrodes to housing are made from tapes. At ISIT the complete process chain starting with the slurry preparation over the tape casting process and the assembly and packaging of complete cells in customized designs is available including also the electrical and thermomechanical characterization. This allows access to all relevant parameters necessary for an optimization process. The electrode and the electrolyte composition up to the cell design can be modified. In addition to the development of prototypes limited-lot manufacturing of optimized cells on a pilot production line at ISIT with storage capacities of up to several ampere-hours is possible. Specific consideration in process development is addressed to the transferability of development results in a subsequent industrial production.

ISIT offers in the field of secondary Lithium batteries a wide portfolio of services:

- Manufacturing and characterization of battery raw materials by half cell as well as full cell testing
- Selection of appropriate combinations of materials and design of cells to fulfil customer requirements
- Application driven housing development
- Test panel
- Prototyping and limited-lot manufacturing of cells

Additional services are:

- Preparation of studies
- Failure analysis
- Testing (electrical, mechanical, reliability, etc.)

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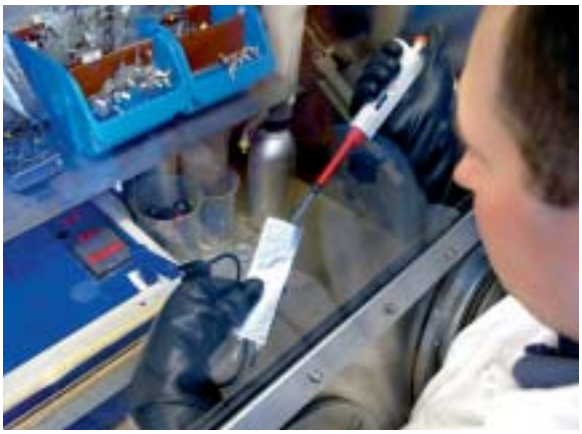
Battery test equipment.

Flexible Lithium polymer battery for wearable electronics. Bottom: Electrode and separator foils.

Prototype of rechargeable Lithium polymer battery for automotive applications. (Above left)

256 channel formation system
for Lithium ion batteries.



Preparation of Lithium polymer battery
in an inert gas atmosphere (glovebox).

Facilities and Equipment

The facilities at Fraunhofer ISIT provide an ideal environment for research & development work as well as for production. In addition to its 150-/200-mm silicon technology line with 2500 m^2 of clean-room (class 1), the institute has a further 450 m^2 of clean-room area (class 100) for specific microsystem processes, including: wet-etching processes, high-rate plasma etching, deposition of non-IC-compatible materials, lithography of thick resist layers, gray-scale lithography, electroplating, microshaping and wafer bonding.

Another 200 m^2 clean-room (class 10-100) is equipped for chemical-mechanical polishing (CMP) and post-CMP cleaning. ISIT also offers non cleanroom labs (1500 m^2) for working groups which develops chemical, biological and thermal processes, electrical and mechanical component characterization, and processes for assembly and interconnection technology.
The ISIT facility also operates a pilot production line for Lithium polymer rechargeable batteries.

Spectrum of Services

The institute offers its services to companies with a wide range of applications, for example medical technology, communication systems, automotive industry, and industrial electronics, based on the specific requirements of the industrial customers for their components or systems. ISIT engineers work in close cooperation with them to design, simulate and produce the components and systems with the specific manufacturing processes.

In this context, ISIT follows the technology platforms concept, which entails defining standard process flows that can be used to manufacture a large group of components simply by varying certain design parameters. Applying this modular technology concept is the optimal way to ensure that ISIT continues to offer competitive prices to its customers. ISIT services have attractive implications for small and medium-sized enterprises, which can take advantage of the institute's facilities and expertise in realizing technological innovations up to products.

Seminar participants in the lead free training line.

Customers

ISIT cooperates with companies of different sectors and sizes.
In the following some companies are presented as a reference:

Aardex, Zug, Switzerland

ABB, Västeräs, Sweden

ABB, Ladenburg

Ablestik, Cambridge, England

Adaptive Photonics, Hamburg

AEMtec, Berlin

Airbus-Systeme, Buxtehude

AJ eBiochip GmbH, Itzehoe

Alcatel Vacuum Technology, Annecy, France

Alma, Lyon, France

Amic, Uppsala, Sweden

Andus electronic GmbH, Berlin

Applied Materials, ICT, München

Arithmatica Limited, Warwick, Great Britain

ARC Seibersdorf Research GmbH, Seibersdorf, Austria

ASE, Seoul, Korea

Atmel Germany GmbH, Heilbronn

Atos Origin, Madrid, Spanien

Atotech Deutschland GmbH, Berlin

Atral, Crolles, France

BASF AG, Ludwigshafen

Basler Securitas Versicherungen, Bad Homburg

Basler Vision Technologies, Ahrensburg

Biont, Bratislava, Slovakia

Bosch, Reutlingen

B. Braun, Melsungen

Bruker Daltonic GmbH, Leipzig

Bundeswehr WTD, Eckernförde

Cardi plus, Sevilla, Spain

Comau S.p.A., Milano, Italy

Condias GmbH, Itzehoe

Conti Temic, Karben

Conti Temic mircoelectronic GmbH, Nürnberg

CTI Ltd, Rotherham, England

DancoTech A/S, Ballerup, Denmark

Danfoss Drives, Graasten, Denmark

Danfoss Silicon Power GmbH, Schleswig

Datacon, Radfeld/Tirol, Austria

Evonik Degussa GmbH, Hanau

Diehl Avionik Systeme GmbH, Überlingen

Digisound-Electronic GmbH, Norderstedt

Dräger Systemtechnik, Lübeck

EADS Deutschland GmbH, Corporate Research Germany, München & Ulm

EN Electronic Network, Bad Hersfeld

Engineering Center for Power Electronics GmbH, Nürnberg

Enitech GmbH, Beutwisch

Equicon, Jena

ESCD, Brunsbüttel

ESW-Extel Systems GmbH, Wedel

EVGroup, Schärding, Austria

EZH GmbH, Bad Hersfeld

Flextronics, Althofen

FOS Messtechnik GmbH, Schacht-Audorf

Freudenberg & Co. KG, Weinheim

Fujitsu Siemens Computers GmbH, Augsburg

GE Healthcare, Helsinki, Finland

GPS GmbH, Stuttgart

Güdel AG, Langenthal, Switzerland

Hannusch Industrieelektronik, Laichingen

Harman & Becker, Karlsbad

H. C. Starck, Leverkusen

Heidenhain, Traunreut

Hella KG, Lippstadt

Honeywell GmbH, Schönaich

HPL S.A., Lausanne, Switzerland

Hymite GmbH, Berlin

IBM Research GmbH, Zürich, Switzerland

IMS, Wien, Austria

INtecs, Boeblingen

Integral Research & Production Corporation, Minsk, Republic of Belarus

Jauch Quartz GmbH, Villingen-Schwenningen

Jungheinrich AG, Norderstedt

Kaco Gerätetechnik GmbH, Kassel

KPS Rinas B.V., Koge, Denmark

Kristronics GmbH, Harrislee-Flensburg

Kuhnke GmbH, Malente

Lam Research, Fremont, USA

Leclanché Lithium GmbH, Willstätt

Lenze Drive Systems GmbH, Hameln

Liebherr Elektronik, Lindau

Litef, Freiburg

Lumio Ltd, Jerusalem, Israel

Mair Elektronik GmbH, Neufahrn

Meder eletronic AG, Engen-Welschingen

Miele & Cie., Gütersloh

M+W Zander, Stuttgart

Nokia Research Center, Nokia Group, Helsinki, Finland

NU-Tech GmbH, Neumünster

NXP Semiconductors, Hamburg

NXP Semiconductors, Nijmegen, Netherlands

Océ-Technologies B.V., Venlo, Netherlands

Omicron Laserage GmbH, Rodgau

Osram Opto Semiconductors GmbH, Regensburg

Oticon A/S, Hellerup, Denmark

Panasonic, Neumünster

PAV Card GmbH, Lütjensee

Peter Wolters GmbH, Rendsburg

PlanOptik AG, Elsoff

Plath Eft GmbH, Norderstedt

Polytec PT GmbH, Waldbronn

Preh GmbH, Neustadt a.d.S.

Prettl Elektronik Lübeck GmbH, Lübeck

Prospektiv Gesellschaft für betriebliche Zukunfts-gestaltung GmbH, Dortmund

Protec Process Systems GmbH, Siegen

Qimonda AG, Neubiberg

Raisio Benecol Ltd, Raisio, Finland

Raytheon Anschütz GmbH, Kiel

Reese+Thies Industrie-elektronik GmbH, Itzehoe

Rehm Anlagenbau GmbH, Blaubeuren-Seissen

Reis Robotics GmbH & Co, Obernburg

Rena Sondermaschinen GmbH, Gütenbach

Robert Bosch GmbH, Salzgitter

Robert Bosch GmbH, Schwieberdingen

Rutronik Elektrische Bau-elemente GmbH, Ispringen

SAES Getters S.p.A., Lainate/Milan, Italy

Sartorius Hamburg GmbH Research & Development, Hamburg

Sauer, Danfoss, Nordborg, Denmark

Saurer GmbH & Co. KG, Übach-Palenberg

Scanbec GmbH, Halle

SEF GmbH, Scharnebek

SensorDynamics (SD), Lebring, Austria

Sensys Traffic AB, Uppsala, Sweden

Siemens AG, Erlangen

Siemens AG, Amberg

SMA Regelsysteme GmbH, Niestetal

Smart Material GmbH, Dresden

SMI, Milpitas, USA

Smyczek, Verl

Solou Laboratories, Berlin

Sonion, Lyngby, Denmark

Sonion A/S, Roskilde, Denmark

Sony Deutschland GmbH, Stuttgart

ST Microelectronics, Crolles, France

ST Microelectronics, Mailand, Italy

Still GmbH, Hamburg

Süd-Chemie AG, Moosbarg

SÜSS Microtec AG, Garching

Technolas, München

Telefonica, Madrid, Spain

Thales, Paris, France

Treichel Elektronik GmbH, Springe

TR-Elektronik, Trossingen

Trinamic, Hamburg

Tronox, Krefeld

Umicore AG & Co., Hanau

Vectron International GmbH & Co. KG, Neckarbischofsheim

Via Electronic GmbH, Hermsdorf

Virion-Serion-Institut GmbH, Würzburg

Vishay Beyschlag, Heide

Vishay, Dimona and Holon, Israel

Vishay Siliconix Itzehoe GmbH, Itzehoe

Vishay Siliconix, Santa Clara, USA

Visual Components Oy, Helsinki, Finland

Vistec, Jena

Volkswagen AG, Wolfsburg

VTT Technical Research Centre of Finland, Espoo, Finland

Wabco Fahrzeugbremsen, Hannover

Wintershall AG, Kassel

Würth Elektronik GmbH, Schopfheim

Innovation Catalogue

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service.

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	Semiconductor equipment manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821 / 17 -4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821 / 17 -4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing, single and double side	Si substrates for device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821 / 17 -4309 gerfried.zwicker@isit.fraunhofer.de
IC processes CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	Detlef Friedrich + 49 (0) 4821 / 17 -4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821 / 17 -4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821 / 17 -4301 detlef.friedrich@isit.fraunhofer.de
Microsystem products	Electronic industry	Prof. Ralf Dudde + 49 (0) 4821 / 17 -4212 ralf.dudde@isit.fraunhofer.de
Ion projection lithography open stencil mask technology and resist processes	Semiconductor industry	Wolfgang Pilz + 49 (0) 4821 / 17 -4222 wolfgang.pilz@isit.fraunhofer.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	Dr. Bernd Wagner + 49 (0) 4821 / 17 -4213 bernd.wagner@isit.fraunhofer.de
Thick epi poly MEMS processing	Sensors and actuators	Dr. Peter Merz + 49 (0) 4821 / 17 - 4513 peter.merz@isit.fraunhofer.de
Piezoelectric microsystems	Sensors and actuators	Hans Joachim Quenzer + 49 (0) 4821 / 17 -4643 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanners and projectors	Biomedical technology, optical measurement industry, telecommunication	Ulrich Hofmann + 49 (0) 4821 / 17 -4553 ulrich.hofmann@isit.fraunhofer.de
Flow sensors	Automotive, fuel cells	Dr. Peter Lange + 49 (0) 4821 / 17 -4220 peter.lange@isit.fraunhofer.de
Microoptical components	Optical measurement	Dr. Klaus Reimer + 49 (0) 4821 / 17 -4233 klaus.reimer@isit.fraunhofer.de
Mastering and replication of micro structures in plastic	Microoptics, microfluidics	Dr. Klaus Reimer + 49 (0) 4821 / 17 -4233 klaus.reimer@isit.fraunhofer.de
Design and test of analogue and mixed-signal ASICs	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821 / 17 -4253 joerg.eichholz@isit.fraunhofer.de
Design Kits	MST foundries	Jörg Eichholz + 49 (0) 4821 / 17 -4253 joerg.eichholz@isit.fraunhofer.de

Product / Service	Market	Contact Person
RF-MEMS	Telecommunication	Dr. Thomas Lisec + 49 (0) 4821 / 17 -4512 thomas.lisec@isit.fraunhofer.de
MST Design and behavioural modelling	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821 / 17 -4253 joerg.eichholz@isit.fraunhofer.de
Electrodeposition of microstructures	Surface micromachining	Martin Witt + 49 (0) 4821 / 17 -4613 martin.witt@isit.fraunhofer.de
Digital micromirror devices	Communication technology	Dr. Klaus Reimer + 49 (0) 4821 / 17 -4233 klaus.reimer@isit.fraunhofer.de
Electrical biochip technology (proteins, nucleic acids, haptens)	Biotechnology, related electronics microfluidics, environmental analysis, Si-Chipprocessing, packaging, chip loading	Dr. Eric Nebling + 49 (0) 4821 / 17 -4312 eric.nebling@isit.fraunhofer.de
Secondary lithium batteries based on solid state ionic conductors	Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde + 49 (0) 4821 / 17 -4307 peter.gulde@isit.fraunhofer.de
Battery test service, electrical parameters, climate impact, reliability, quality	Mobile electronic equipment medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde + 49 (0) 4821 / 17 -4307 peter.gulde@isit.fraunhofer.de
Quality and reliability of electronic assemblies (http://www.isit.fraunhofer.de)	Microelectronic and power electronic industry	Karin Pape + 49 (0) 4821 / 17 -4229 karin.pape@isit.fraunhofer.de
Material and damage analysis	Microelectronic and power electronic industry	Dr. Thomas Ahrens + 49 (0) 4821 / 17 -4605 thomas.ahrens@isit.fraunhofer.de
Thermal measurement and simulation	Microelectronic and power electronic industry	Dr. M. H. Poech + 49 (0) 4821 / 17 -4607 max.poech@isit.fraunhofer.de
Leadfree / RoHS transformation in electronic assembly	Electronic industry	Dr. Thomas Ahrens + 49 (0) 4821 / 17 -4605 thomas.ahrens@isit.fraunhofer.de
Packaging for microsystems, sensors, multichip modules (http://www.isit.fraunhofer.de)	Microelectronic, sensoric and medical industry	Karin Pape + 49 (0) 4821 / 17 -4229 karin.pape@isit.fraunhofer.de
Wafer level packaging, ultra thin Si packaging and direct chip attach using flip chip techniques	Microelectronic, sensoric and medical industry, automotive industry	Dr. Wolfgang Reinert + 49 (0) 4821 / 17 -4617 wolfgang.reinert@isit.fraunhofer.de
Vacuum wafer bonding technology	Microelectronic, sensoric and medical industry, automotive industry	Dr. Wolfgang Reinert + 49 (0) 4821 / 17 -4617 wolfgang.reinert@isit.fraunhofer.de

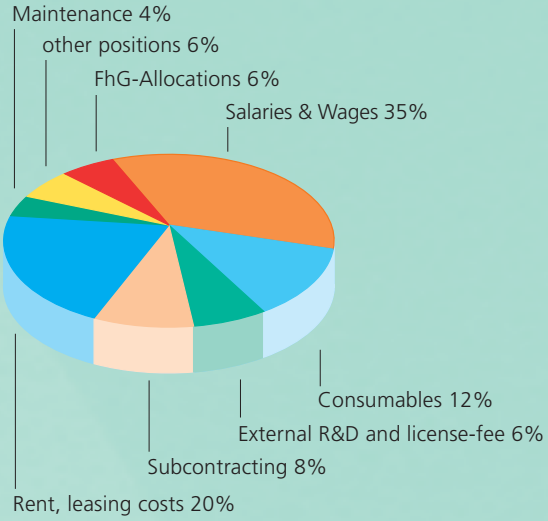
Representative Figures

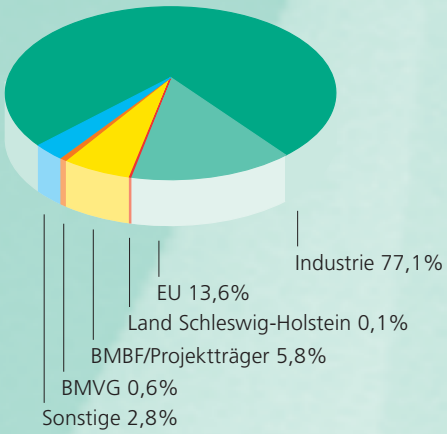
Expenditure

In 2007 the operating expenditure of Fraunhofer ISIT amounted to 18.884,9 T€. Salaries and wages were 6.487,3 T€, material costs and different other running costs were 12.397,6 T€.

Income

The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to 12.498,2 T€, of government/project sponsors/federal states amounting to 1.057,3 T€, of European Union/others amounting to 2.661,9 T€ and basic funding of 2.667,5 T€.



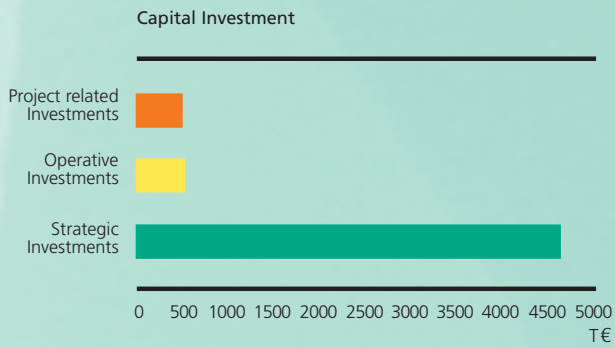


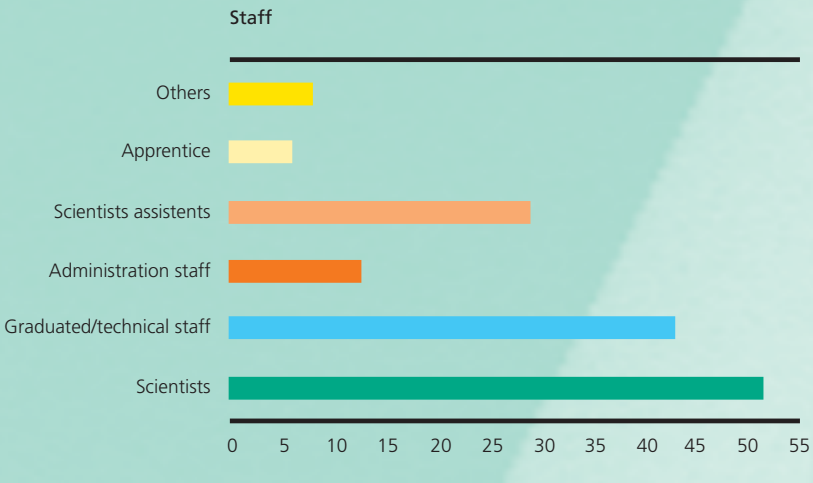
Capital Investment

In 2007 the institutional budget of capital investment was 5.602,3 T€. The amount of strategic investment was 4.608,4 T€, the operating investment was 516,0 T€ and project related investments were amounted to 477,9 T€.

Staff Development

In 2007, on annnual average the staff consisted of 106 employees. 51 were employed as scientific personnel, 43 as graduated/technical personnel and 12 worked within organisation and administration. The employees were assisted through 29 scientific assistents, 5 apprentices and 7 others.





The Fraunhofer-Gesellschaft

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration. The organization also accepts commissions from German federal and Länder ministries and government departments to participate in future-oriented research projects with the aim of finding innovative solutions to issues concerning the industrial economy and society in general.

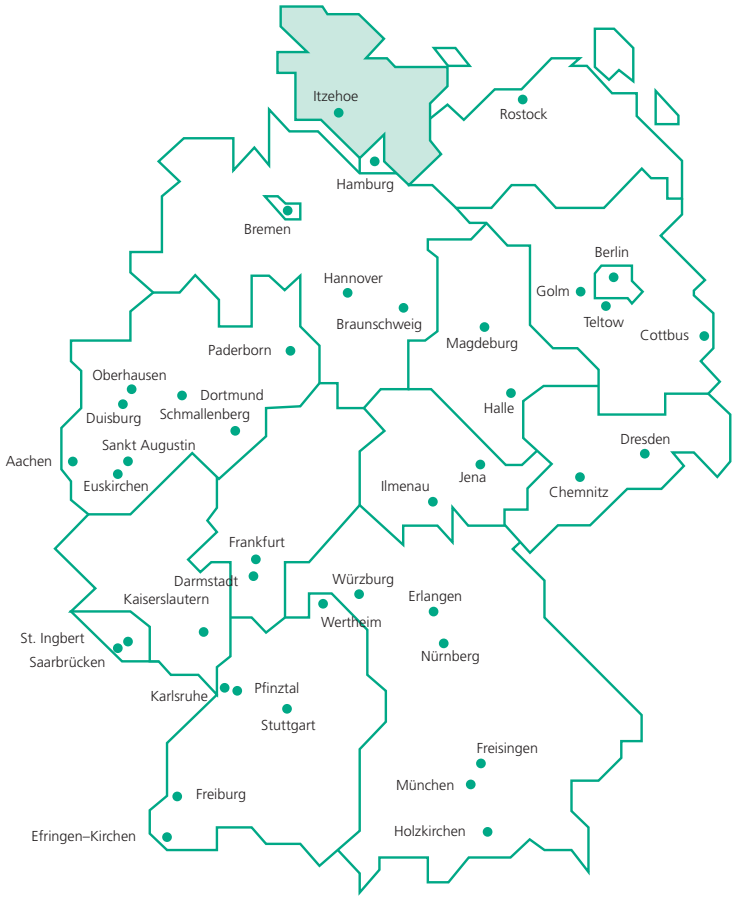
Applied research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, accelerating technological progress, improving the acceptance of new technologies, and not least by disseminating their knowledge and helping to train the urgently needed future generation of scientists and engineers.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, in other scientific domains, in industry and in society. Students working at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

At present, the Fraunhofer-Gesellschaft maintains more than 80 research units, including 56 Fraunhofer Institutes, at 40 different locations in Germany. The majority of the 13,000 staff are qualified scientists and engineers, who work with an annual research budget of 1.3 billion euros. Of this sum, more than 1 billion euros is generated through contract research. Two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Only one third is contributed by the German federal and Länder governments in the form of institutional funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

Affiliated research centers and representative offices in Europe, the USA and Asia provide contact with the regions of greatest importance to present and future scientific progress and economic development. The Fraunhofer-Gesellschaft is a recognized nonprofit organization which takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

Locations of the Research Establishment



Representative Results of Work

Power-Electronics for Higher Energy Efficiency

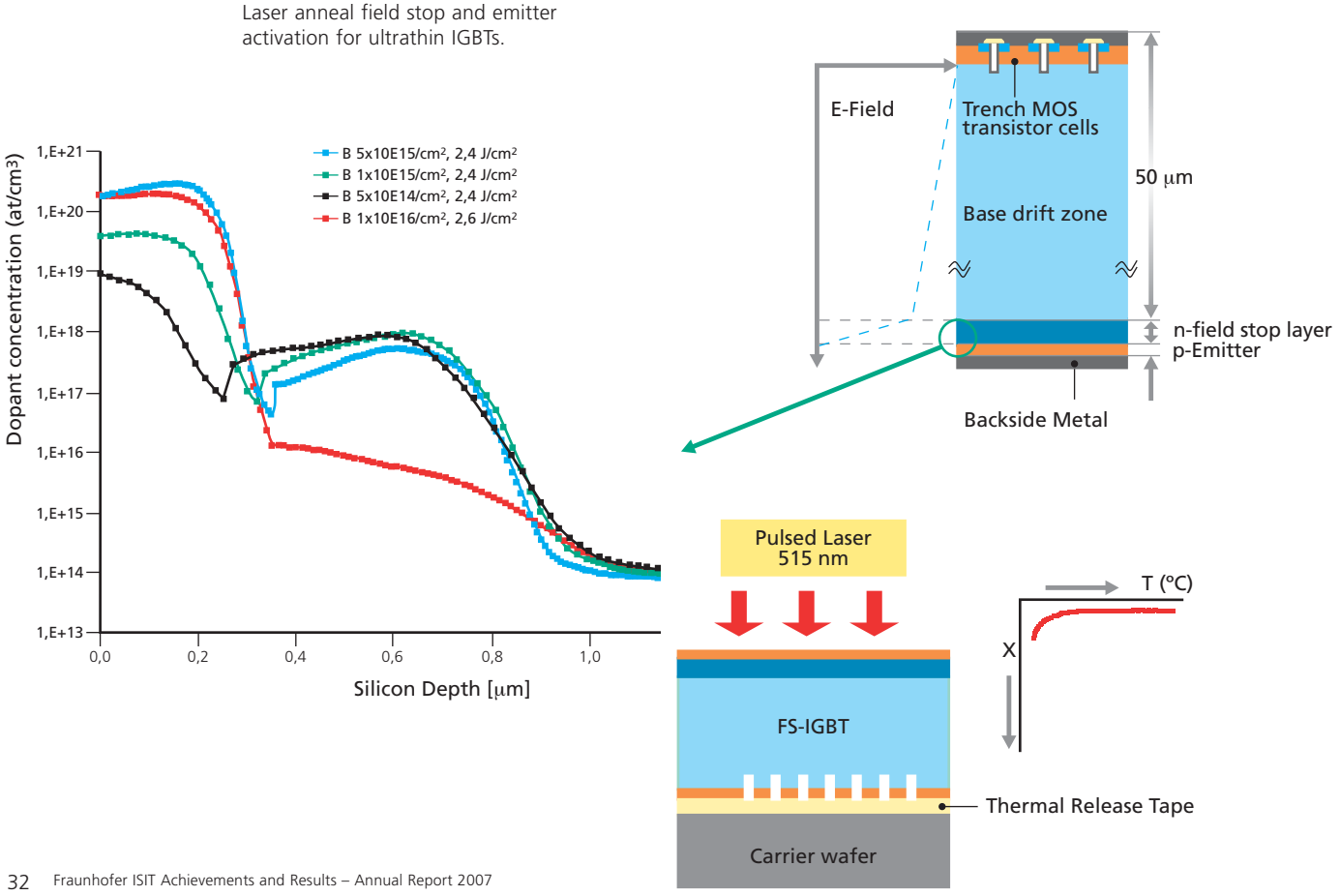
Limited resources for fossil primary energy and higher energy consumption world wide is already leading to significant increase of the energy costs and will further rise up in future. Renewable energy sources will increase its contribution to the energy supply, but however will not compensate for the growing demand of energy in total. Independently on the future development of the world wide energy distribution the improvement of energy efficiency will be the main topic in power electronics for the next decades with annual growth rates of 10 % and more.

Within the entire energy supply chain from the primary energy source via electrical energy conversion in power plants down to the equipment of the end user the power electronics will help to increase efficiency.

The potential of energy saving by use of power electronics can be impressively demonstrated in two large fields of energy consumption, namely industrial motor drives and lighting. Two third of the electrical energy in industry is needed for motor drives only. In Germany the use of speed controlled energy efficient motors can save more than 15 % of this energy which amounts in total to 27 TWh per year (ZVEI; Zentralverband der Elektrotechnik und Elektroindustrie). In case of lighting the potential for energy saving is estimated with yearly 11 TWh (ZVEI) which is more than 2% of the total electrical energy consumption per year in Germany.
This amount of energy savings is equivalent to 11 power plants with 400 MW each and is just covering approx. two third of the total saving potential of electrical energy.

Power electronics is the key issue and thereunder especially the discrete power semiconductor devices. Next to the efficiency improvement for existing applications new markets are growing up also. Here the automotive sector is most challenging since it becomes clear that within the next decades the electrical power train will become a real alternative to combustion drives.

Figure 1:
Laser anneal field stop and emitter activation for ultrathin IGBTs.



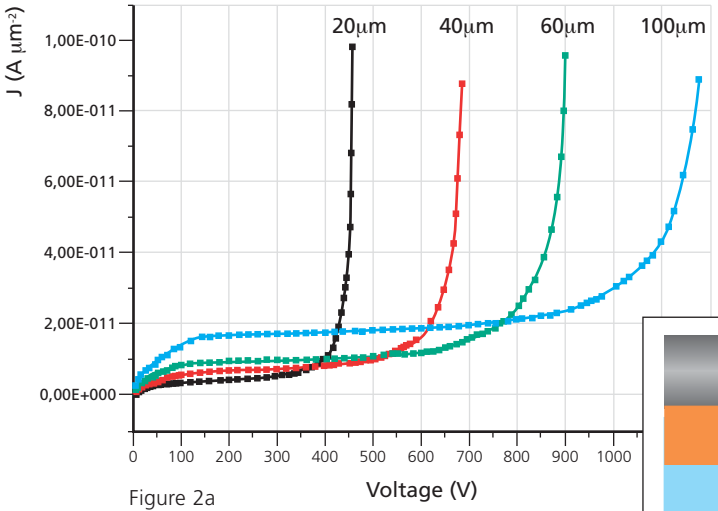


Figure 2a

Figure 2b

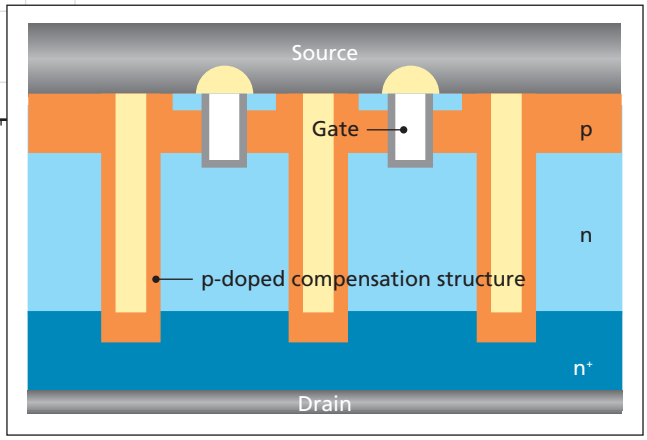


Figure 2:
a) Principle schematic of a trench based charge compensation PowerMOS transistor.
b) The I-V characteristic shows the simulated blocking behaviour for different trench depths.

The total sales in 2007 for Hybrid Electrical Vehicles was in the range 600 000 cars with projected 2 Million cars in 2010. This is leading to a growing market for high performance power devices with annual growth rate of > 15 % for the two dominant types of semiconductor devices IGBTs (Insulated Gate Bipolar Transistors) and PowerMOS transistors.

The overall demand for energy efficient components in power electronics is initiating an increasing need for R&D also. Therefore ISIT is focussing on R&D topics related to new power semiconductor devices. Excamples are given in the following:

- Development of new energy efficient semiconductor power devices
- Adaptation of power semiconductor devices for new packaging techniques

For the IGBT development the investigation of laser annael field stop devices is of specific interest. New handling concepts for ultrathin IGBTs with 50 µm substrate thickness capable for backside laser annealing have been evaluated. For this purpose screening of implantation parameters for the backside field stop and emitter layer as well as appropriate laser anneal parameters were investigated. The variation of emitter implantation parameters at a laser energy density of 2,4 J/cm^2 is depicted in figure 1 showing the spreading resistance doping profiles for the field stop and emitter layers. The laser activated Phosphorous field stop dose was found to be suffiicently high for all Boron doses in the range 5x 10^{14} – 5x 10^{15} cm^{-2}.

For the PowerMOS transistors the reduction of R_{Dson} is the most important R&D topic for minimizing the conduction losses. Especially for MOSFETs in the voltage range below 50 V with

high cell densities the substrate thinning is most effective for R_{Dson} reduction. A handling concept based on the temporary bonding by use of thermal release tapes was verified for sub-50 µm substrate thicknesses. A reduction of R_{DSon} by 40 % could be demonstrated for 20–30 V PowerMOS transistors with the potential for further improvement.

A significant improvement of R_{Dson} for high voltage PowerMOS transistors in the voltage range > 150 V is possible only with charge compensation devices. Here, ISIT is developing trench based super junction transistors. Compared to standard devices a R_{Dson} reduction by a factor 6 down to 5 mOhmcm² is expected for e.g. 300 V PowerMOS transistors.
The principle of the trench based compensation device is shown in figure 2a. The p-doped vertical column is located around the trench edges for compensating the drift zone charge in the blocking state. The doping concentration of the drift zone is increased by a factor of 10 compared to standard devices.

Figure 2b shows the simulated reverse bias I-V characteristic for different trench depths. For a 300 V super junction device a trench depth of approx. 20 µm is required.

With the performance improvement of power semiconductor devices the packaging of power devices has to be improved also. A new packaging concept with low parasitic resistances and inductances as well as an improved heat transfer is mandatory in order to benefit from the performance gain of the power devices. The principle of such a packaging concept is shown in figure 3 illustrating a sandwich type Direct Copper Bond (DCB) stack having the power devices assembled in between by front and back side soldering. No standard wire bonding is needed anymore since wire bonds can contribute to the total R_{DSon} value in the mOhm range. The assembly is low inductive and the heat ransfer can be directed to the top and bottom of the sandwich structure.

The power devices however have to be adapted for the wire less assembly. This can be done by modification of the final chip metalisation in order to realize a solderable front side metalisation. As shown in figure 4 a solder bumping process based on ball placement is completing the IGBT back end process.
A Cu based Under Bump Metallisation (UBM) was used. The implementation of a bumping process into an entire process scheme of ultrathin discrete power devices is an actual research topic.

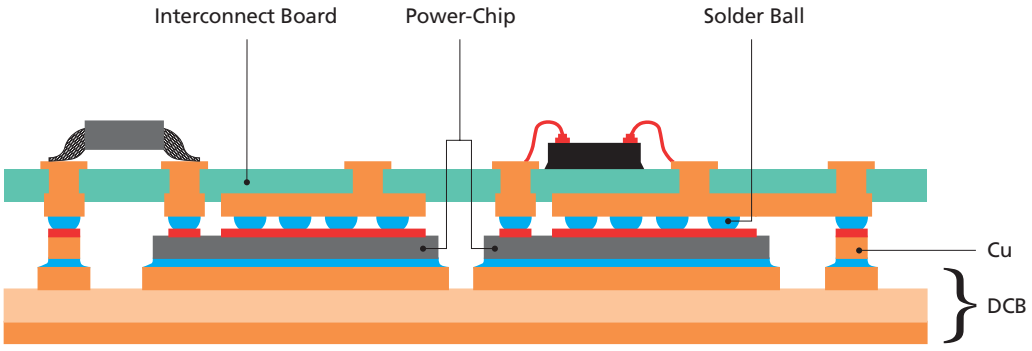


Figure 3:
Principle schematic of a sandwich type power module assembly. The power devices are soldered at the front and back side.

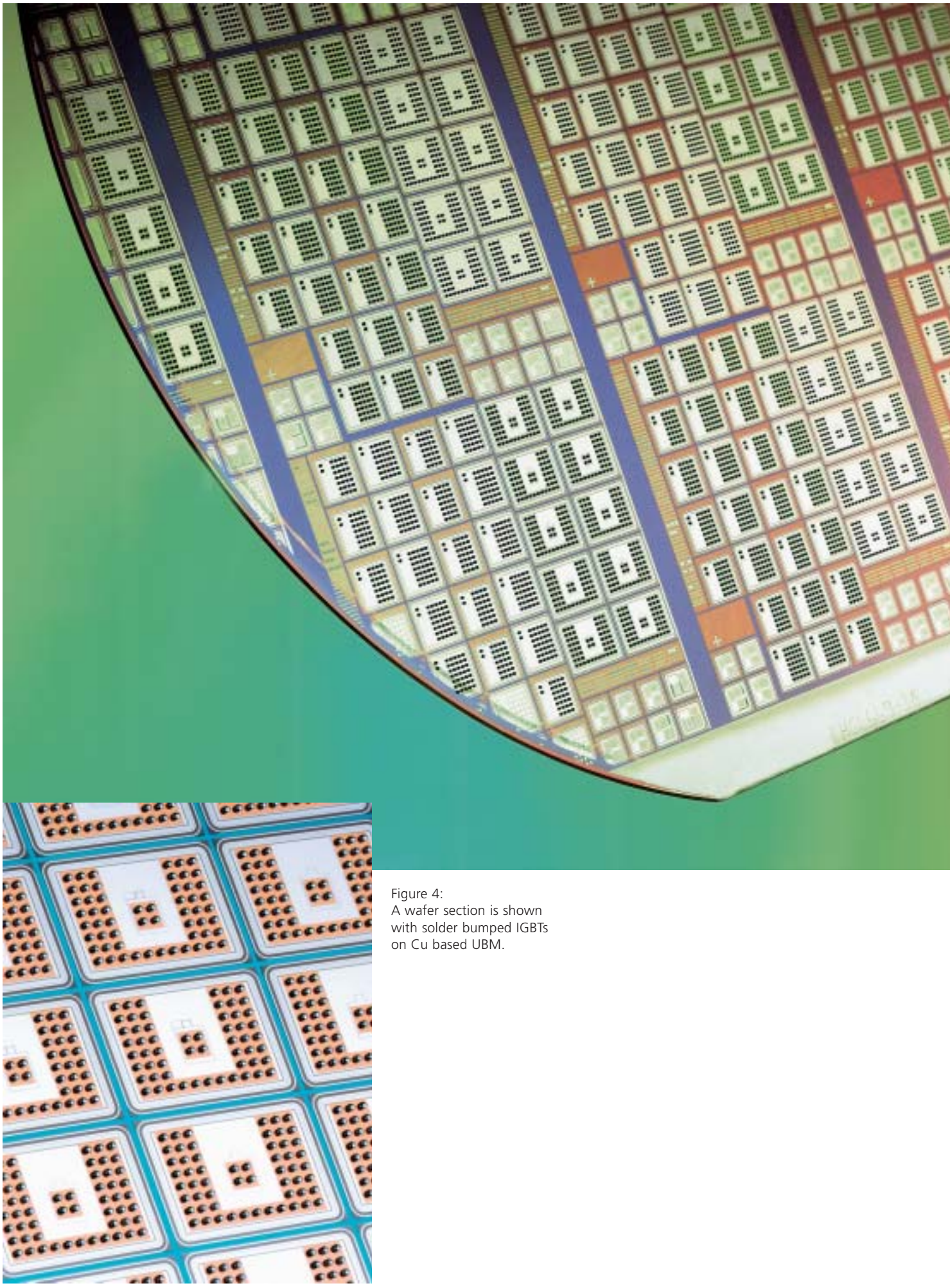


Figure 4:
A wafer section is shown with solder bumped IGBTs on Cu based UBM.

Lithography and Galvano Plating in Thick Resist Layers

Lithography for thick resist layers is prerequisite for many processes in MEMS and advanced packaging applications. The key process is the metal deposition by electro plating within patterned thick resist structures. This technique is well established and widely used for surface micro machining, when thick metal structures have to be deposited, mostly Ni, Cu or Au material. The principle process sequence is illustrated in figure 1 beginning with the sputter deposition of a seed layer and a subsequent lithography process for a thick photo resist. After galvanic growth the photo resist is removed as well as the exposed seed layer by ion milling or wet chemical etching.

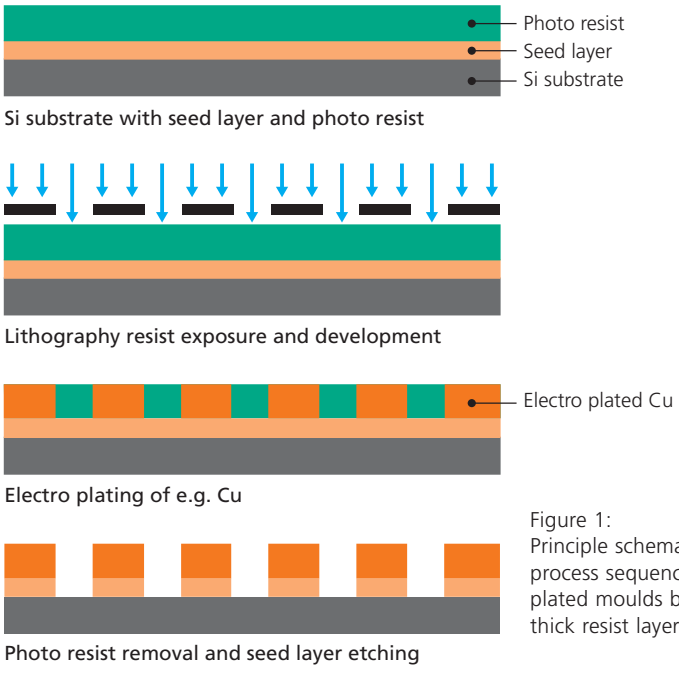


Figure 1:
Principle schematic of the process sequence for electro plated moulds by use of thick resist layers.

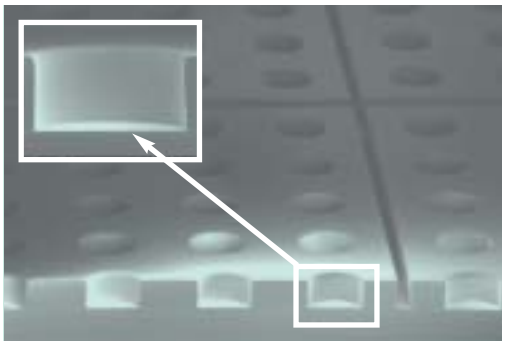


Figure 2:
Different test features in XP 5590 photoresist with a height up to 120 µm.

The maximum standard resist thickness for this purpose is currently in the range of 50 µm. If resist layers with higher thicknesses are required double or triple spin coating with subsequent exposure and development steps have to be applied so far.

In the following results of a new photo resist process are demonstrated which have been evaluated in a single lithographic sequence. Preferentially, lithography consists of well established steps, i.e. spin coating, UV exposure and immersion development. A negative tone resist was developed by Rohm & Haas (XP 5590) with promising new application feature:

- thickness after spin-coating in the range of 150 µm
- near vertical side wall after exposure and development, aspect ratio ~ 2
- soluble in organic solvents after galvano plating

Especially, the last item eliminates the need of any aggressive plasma stripping process. The resist itself consists of a Polyacrylate backbone and can be handled on standard coater developments tools. The development in aqueous solution of Tetra-Methyl-Ammonium-Hydroxide (TMAH) provides an easy application as well.

As shown in figure 2, excellent resist structures could be achieved which are suitable as moulds for galvano plating processes. The profile of the resist edges exhibit a slight negative slope which is typical for negative tone resists. The exposure process was carried out with a Suess mask aligner having a special optic for thick resist processing. Using a fountain plater from the RENA galvano clustertool copper pillars have been grown up to a height of 120 µm. Special care had to be taken to enable nucleation on the plating base. A moderate oxygen plasma

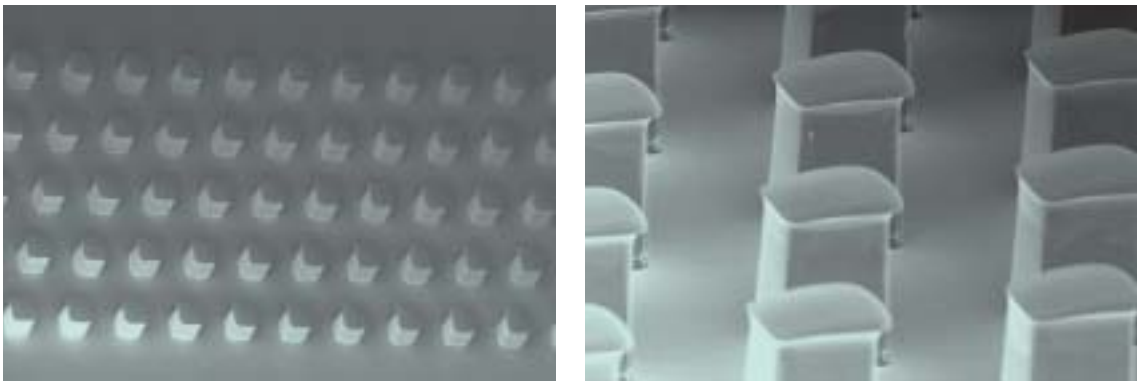


Figure 3:
Array of Cu pillars
120 µm in height.

stripping process served as descum, removing some resist residuals from the bottom of the grooves. If pre-processed correctly, the resist didn't show any crack formation or peeling off.

The figures 3 indicate some examples of a test pillar array where the resist was removed previously. According to the demands mushroom like studs or flat pillars can be obtained.

A further application for galvano plating based on thick resist moulds is the wafer level chip size packaging (WLCSP). Here, the plating of Sn or Sn alloys (Sn-Ag) for solder bump formation is used for e.g. fine pitch bumping purposes (< 100 µm) in high integration packaging processes. Solder plating is an alternative to solder paste printing when the geometrical requirements of the bumps are beyond the limits of screen printing. The combined galvano plating of the Under Bump Metallisation (Ni UBM) followed up by the Sn solder bump plating is beneficial for the reduction of the process complexity. The principle of solder bump formation based on Sn-Ag plating is depicted in figure 4. After plating, resist and seed layer removal the typical solder bump shape was formed by solder reflow. The cross sections are showing Sn-Ag solder bumps of 80 µm in height with a Ni-UBM layer underneath.

The lithography process for the new thick resist has the potential to extent the resist thickness up to 150 µm without using double coating-expose-development or resist types which require a release layer.

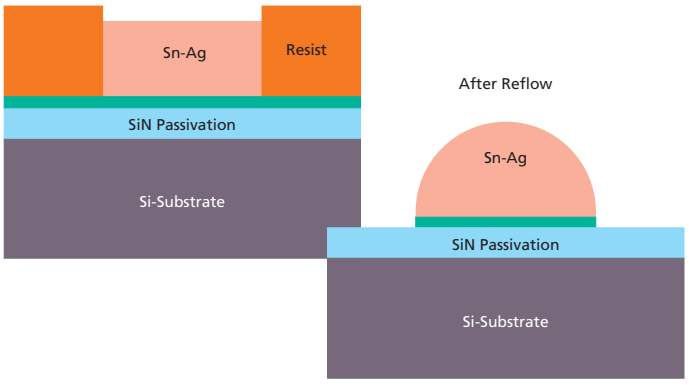
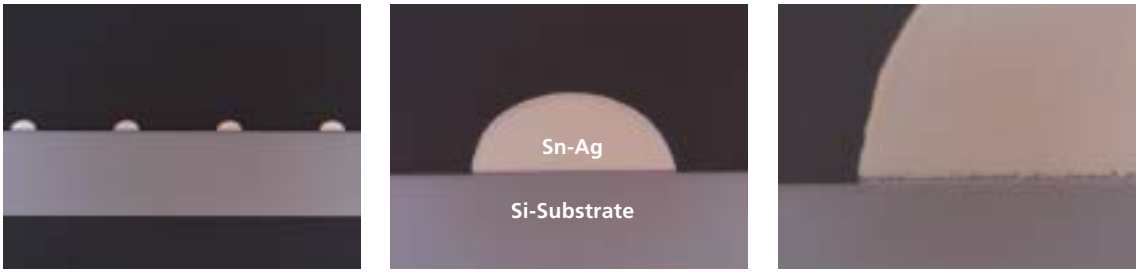


Figure 4:
Galvano plating of Sn-Ag as an alternative process to solder paste printing.



Sensor Pinpoints Leaks in Water Lines

Researchers at the Fraunhofer ISIT and their colleagues at SensorDynamics (Pisa, Italy) have developed silicon-based water flow sensors that can detect leaks in municipal freshwater pipeline systems at a fraction of the cost of conventional flow sensors.
The statistics are alarming. Because aging municipal pipes - some over 100 years old - have holes or fissures, up to 40% of fresh water flowing through supply lines today never reaches the end consumer, but seeps out of leaky pipes into the ground. To date there are no cost-efficient ways to detect these leaks. Conventional high-end flow sensors, which can cost anywhere from 1,000 to 2,000 € per sensor, are too expensive to be used throughout entire networks.

Working with Pisa's water supply company, Acque S.p.A., researchers are testing the new probes, which utilize microelectromechnical (MEMS) technology and draw on the same principles as mass air flow sensors that measure the air intake in car engines. Now ISIT researchers are able to use these sensors in liquids for the first time. During initial testing, the sensors survived for three months under water without suffering any damage.
Central to the probe design is a sensor chip that features two heating wires mounted one behind the other within a thin silicon membrane ~2 µm thick. An electric current flows through the wires and heats them to a constant temperature of ~50°C. When cold water flows over the sensor, it cools the front wire and energy from that wire

Figure 1:
This image of a water sensor prototype illustrates the components of the sensor chip located at the end of a pipe.

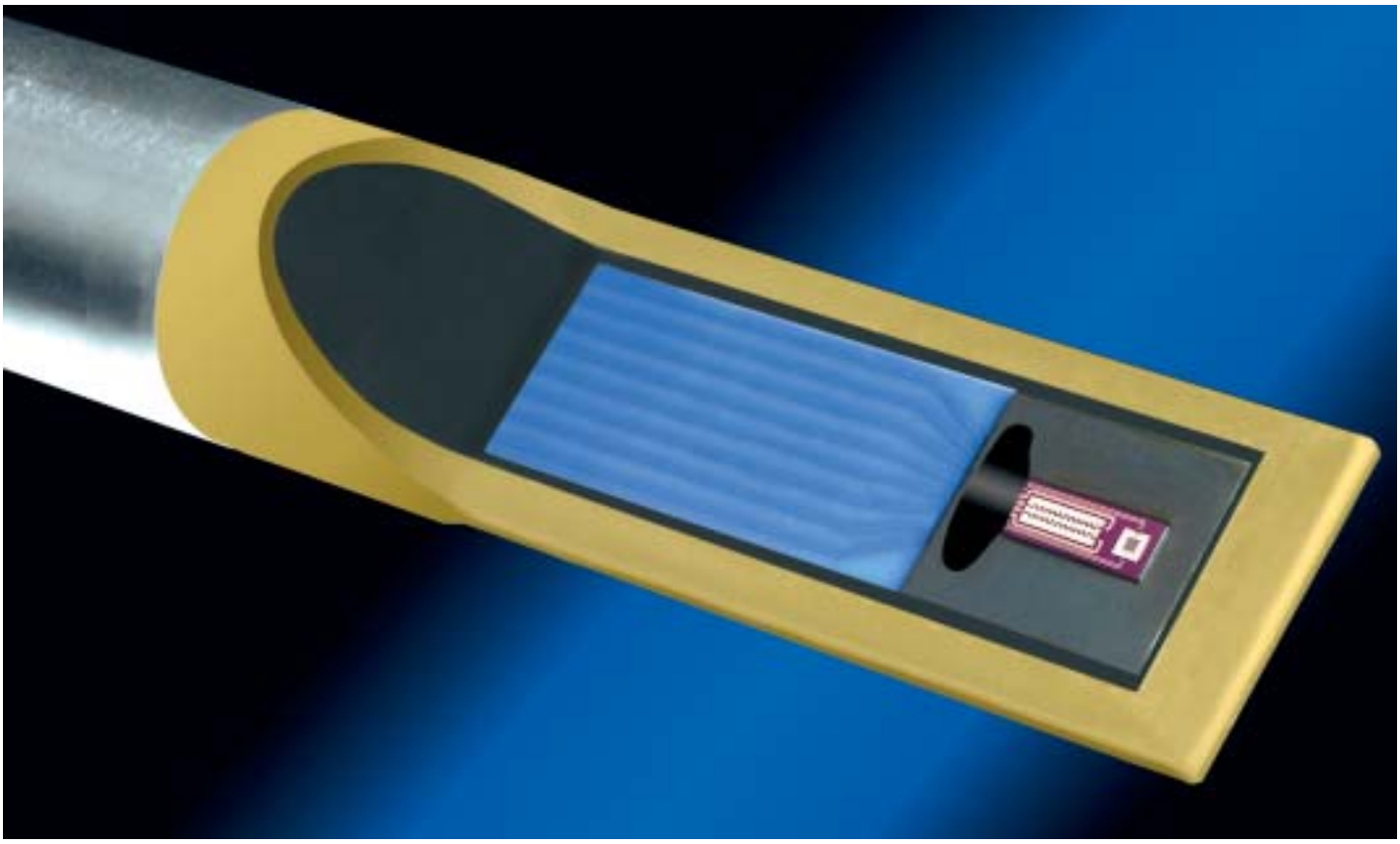


Figure 2:
Typical application for water network monitoring.

Figure 3:
Acque s.p.a. corporate headquarter in pisa.

warms the water flow. Subsequently, warmer water flows over the rear wire and lessens the cooling effect to the rear wire.
As the wires' temperature drops, their resistance drops, which allows more electric current to flow into the wires to keep their temperature constant. Based on the difference in electrical current needed to maintain the front and rear wires' temperature, researchers are able to determine the speed and volume of the water traveling over the sensor. The difference in electrical current between the two wires can determine the direction of the water flow as well. If the difference between the front and rear wire is positive, it indicates the water is flowing in one direction. A negative difference indicates water is flowing in the other direction.
A special feature of this sensor is its ability to operate in pulse mode. Since the wires are not heated constantly, but only for about three seconds out of every minute, they are cold most of the time. This helps to reduce lime deposits and air bubbles that could otherwise distort the measurements. Pulsed operation also saves energy, which promotes longer battery life.
Another advantage with the MEMS technology is that one silicon wafer can hold up to 500 of sensor chips. The chips will be manufactured in a metal oxide semiconductor (Power-MOS) transistor line using predominantly standard integrated circuit processes. This ensures the chips can be produced in large quantities with guaranteed uniformity, a factor that is critically important for many applications.
To create the prototypes used for the Pisa field test, researchers mounted a silicon chip on a ceramic substrate and place it at the end of a 21 mm stainless steel (SS) pipe. Also located within the pipe are the sensor system's signal evaluation circuit, a memory chip that stores the sensor data, and small AAA-type alkaline batteries that supply power for these components. Currently the reliability of the sensor system is being tested in a water supply station in Pisa, where the researchers installed a number of sensor prototypes into the water pipes at central distribution points around the end of November 2007.
Holes were drilled into the water supply pipes, and the sensors were inserted with just the silicon-chip on ceramic end submerged in the water flow. The water lines did not need to be shut down during the installation process.
During testing, which is expected to conclude sometime in 2008, the sensors must withstand the water flow for several months at full operation. Also, a parallel comparison with conventional flow sensors is implemented.
When starting the leak detection test, researchers will calculate the real water flow. Then they will record measurements between two sensor points on the pipeline. Mass will be calculated as L/s and velocity as m/s. In a closed network, the velocity of the water traveling from one sensor to another should be the same. If there is a leak, the mass of water is reduced - which, in turn, decreases the velocity. So a change in the mass flow indicates a leak in the system.
For the duration of the testing phase, the sensors will include a USB connection so the researchers can collect sensor data with a laptop computer. Ultimately, data from the sensors will be transmitted so that it can be retrieved by mobile phone or radio.

Improvements of Wafer-Level Vacuum Packaged Micro-Scanning Mirrors for Laser Projection Displays

Driven by a growing interest in portable projection displays for cell phones, digital cameras, PDAs, game consoles etc. silicon based scanning micromirrors become increasingly attractive. Synchronized to the modulation of a RGB laser source these micromirrors enable high resolution full colour image projection by scanning a laser beam horizontally and vertically across the projection screen.
Fraunhofer ISIT is supposed to be the first to have introduced hermetic wafer level packaging of two-axis scanning micro-mirrors for laser projection. Hermetic wafer-level packaging of optical micro-electro-mechanical systems (MEMS) is essential to protect the sensitive devices against contamination by particles, fluids or gases.
It is a prerequisite for the high volume mass producibility that is required by consumer applications like laser projection displays for cell-phones. A special glass wafer that provides deep cavities and optical windows of required quality is anodically bonded on top of the MEMS mirror wafer. An additional wafer provided with a getter thin film is eutectically bonded from backside and thus enables vacuum operation of the scanning micro-mirror. Applying a Titanium thin film getter leads to a cavity pressure well below 10 mTorr. Thereby, quality factors higher than 200 000 have been achieved, enabling high frequency and large angle scanning at very low driving voltages (figure 1). The maximum scan angle is limited only by the fracture strength of the torsional suspensions and can exceed 50 degrees in both axes even at frequencies higher than 30 kHz. The current mirror designs target SVGA-resolution in Lissajous projection mode and provide fast axis scanning that meet the requirements for XGA-raster-scanning projection. But there also exists an inevitable drawback of packaged scanning micro-mirrors: The glass surfaces generate reflexes that are visible as bright spots directly centered in the projected image. To avoid such a distortion the mirror now can be statically and permanently pre-inclined by 15 degrees within the wafer level packaging process. That is enabled by an auxiliary frame that surrounds the two axis scanner (figure 2). By means of this tilt the reflexes can be spatially separated from the projected image.

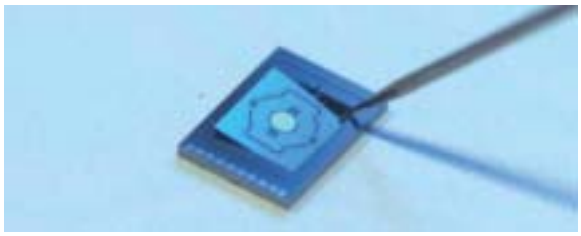
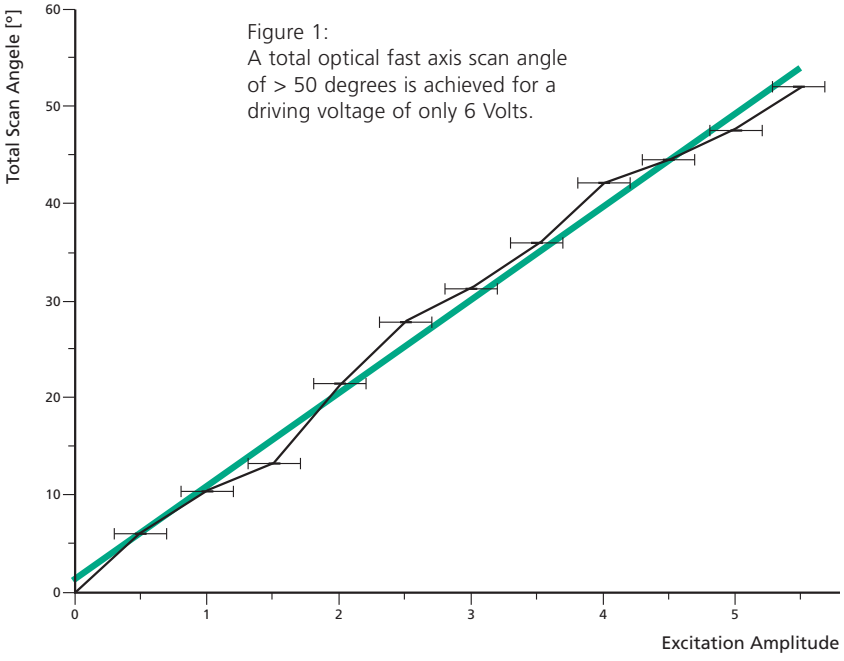


Figure 2: A new mirror design enables permanent static preinclination of the 2D-scanner for spatial separation of reflex and projected image.

Figure 3: Scanning laser image projection.

Figure 1:
A total optical fast axis scan angle of > 50 degrees is achieved for a driving voltage of only 6 Volts.



Wafer-Level Packaging of RF-MEMS

Radio frequency MEMS switches promise to combine the high performance and low power consumption of common mechanical microwave switches with the small size, weight and low cost of semiconductor devices. For example, substantial improvements of functionality and power efficiency are expected for wireless communication systems like cell phones from the introduction of MEMS based programmable impedance matching and signal filtering.

However, RF MEMS switches are a very complex challenge from a technological point of view. One of the main problems is the packaging. RF MEMS switches must be sealed hermetically to protect them from environmental influences and to ensure a stable atmosphere during the entire lifetime. Since the free standing switch structure usually consists of highly conductive metals like aluminium, the packaging temperature must be limited to 300°C to avoid mechanical degradation. At the same time cost, size and height are crucial requirements in the case of cell phone components. Consequently, all MEMS devices processed on a wafer must be capped simultaneously in one step like it is provided by wafer-to wafer bonding techniques. To allow low cost MEMS fabrication the sealing process must tolerate a certain level of topography. Subsequent thinning of the bonded wafer stack and singulation must be possible using standard procedures of IC technology.

On behalf of NXP Semiconductors at Fraunhofer ISIT an efficient wafer-level packaging process for RF MEMS switches has been developed based on AuSn eutectic bonding. Buried lateral feed-throughs are used to connect the MEMS to the outside, see figure 1. Only three lithography steps are required to fabricate the silicon cap wafer with cavities surrounded by AuSn sealing frames. Corresponding Au sealing frames are fabricated on the MEMS wafer using one more lithography step. After release of the MEMS structures the wafers are joined at 300° C under a well defined atmosphere using standard bonding equipment. The bonding process is compatible with the Al alloy based RF MEMS switches from NXP. Reliable, strong and hermetic joints have been demonstrated on 6" wafer level. A sealing width of only 80 µm in combination with optimised bond frame crossings ensure a good RF performance in the frequency range for mobile communication.

Figure 1:
Schematic cross-section through the wafer stack with the packaged MEMS switches after cap dicing.

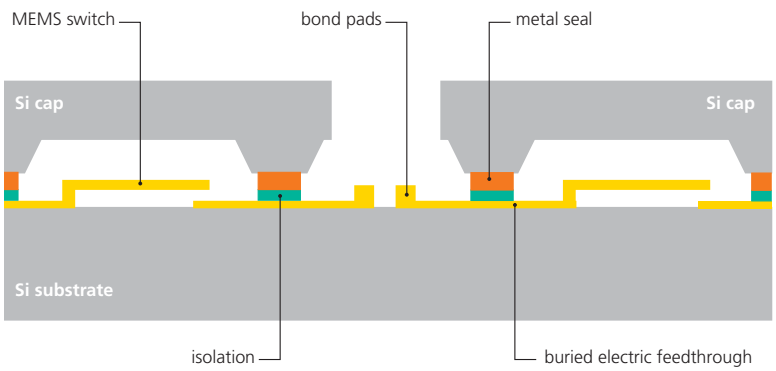
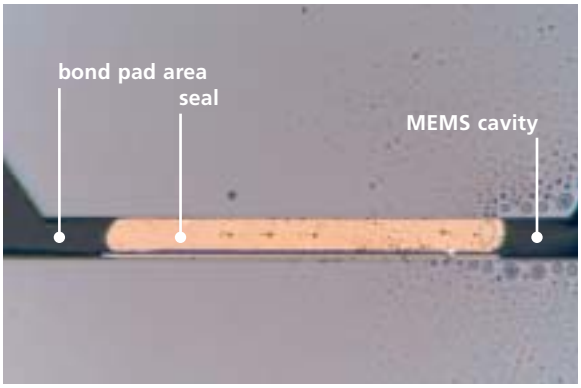


Figure 2:
Cross-section of the bonded wafer pair showing the AuSn sealing layer.



Reliability and Robustness of MEMS Devices

MEMS technology has shown its maturity by overwhelming performance at low cost. Present mass products like surface micromachined inertial sensors have achieved market breakthrough in applications such automotive (air bag, ESP), entertainment (game pads), electronics (harddisk protection) or life science applications (bio-monitoring). Having solved the primary device specifications the focus of research activities emphasizes secondary aspects like reliability and robustness issues.

Table 1:
Main standard qualification tests for electronic devices (AEC-Q100, MIL-STD-883).

Environmental Impact	Accelerated Life Time Test
Temperature	Burn-In / Early life time failure High temperature operating life time Temperature cycling Thermal shock
Moisture Corrosion Chemical attack	Humidity storage Pressure cooker Dew point Salt
Mechanical shock load	Drop test (1 m)
Electrostatics	Electrostatic discharge test
Hermeticity	Package integrity Fine/Gross leak test

Table 2:
Enhanced MEMS specific reliability and robustness tests.

Environmental Impact	Accelerated Life Time Test
Mechanical load	Micro tensile strength (shear strength) Micro shear strength Micro chevron strength Cyclic load strength (fatigue)
Mechanical shock load	Calibrated drop test (fracture strength) Static stiction test
Mechanical vibration	Vibration impact near device resonance In-use stiction
Temperature Hermeticity Humidity	Electrical wafertest / vacuum prober Fine leak test for nanoLiter packages on wafer level Resonant measurement of surface charges

The assurance of the device life time and the resistance against mechanical or chemical impact is more and more a key element for successful MEMS products. In case of surface micromachined vibrating gyrometers the operating frequency nowadays may exceed 10 kHz which equals a lifetime cycle load of up to 10^{12} cycles over 17 years. Applied shock loads e.g. by accidental dropping can result in a mechanical impact of up to 100000 g which implicates potential damage on fragile MEMS structures. This trend for higher reliability and robustness properties are often in contradiction to ongoing miniaturization and higher performance of MEMS devices. In addition an extensive protective housing is not accepted for cost or size reason. Consequently the long term stability of the used materials must be predictable therefore potential failure modes must be known and determined.
For electronic and microelectronic components like ASICs there are standardized test conditions present like the AEC-Q100 or MIL-STD-883 (table 1), which include accelerated life time testing under temperature or humidity stress. For MEMS however these proposed test conditions are insufficient since they do not account for the mechanical degree of freedom which MEMS comprises. Therefore adequate experimental test equipment and standards for MEMS devices are needed.
For the characterization of reliability and robustness of MEMS devices Fraunhofer ISIT provides a broad set of test equipment and processes depicted in table 2.
A calibrated high-g shock stand simulates the impact of mishandling, unintended dropping or machinery induced shock load. The high acceleration impact leads to destruction especially in areas of local stress concentration (see figure 1). On test devices the stress distribution was designed for predetermined breaking points so the line of fracture and crack propagation can be explored and underlined by appropriate theoretical modelling.
Wear and abrasion occur also on a microscale level when movable structures come to contact. In case of continuous mechanical impact on

Figure 1:
Broken poly silicon beam after high shock impact of 30000 g.

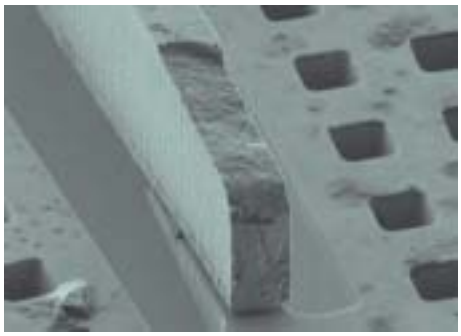


Figure 2:
Poly silicon anchor with silicon debris effected from in-use abrasion and wear.

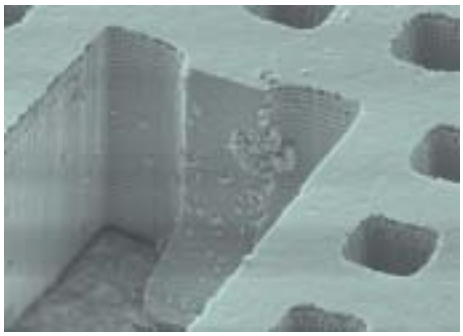
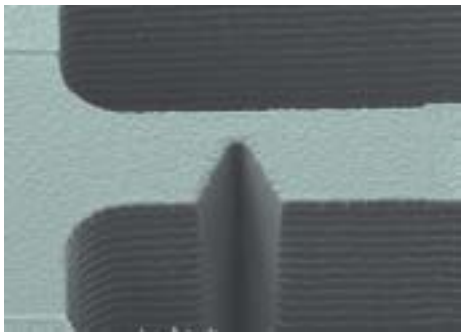


Figure 3:
Accelerated fatigue test beam with sharp micro notch to enhance mechanical stress impact.



silicon structures the material attrition effects nanoscaled particles as seen with high resolution scanning electron microscopy in figure 2.
The development of protective thin film hard coatings for high wear resistance can hereby be monitored directly.

In a dedicated shaker test stand a mechanical acceleration up to several hundred g is impinged on MEMS devices under operation. The superposition of the high velocity operational in-plane movement with out-of-plane vibrational excitation leads to hard contact incidences of opposite devices surfaces. Local energy dissipation and adhesion forces may lead to permanent adherence. This effect is called stiction in-use and may constrain the potential field of application of MEMS devices. The quantitative analysis of the stiction-in-use behaviour is of great importance and enables the evaluation of sticking robust designs, materials or processes.
For lifetime prediction and fatigue mechanism determination the cyclic load strength of vibrating structures can be measured in a chip-level mini vacuum chamber. For accelerated testing the mechanical stress concentration in test beams is drastically enhanced by micro notches (see figure 3). Monitoring of frequency and motion amplitude is used for indicating

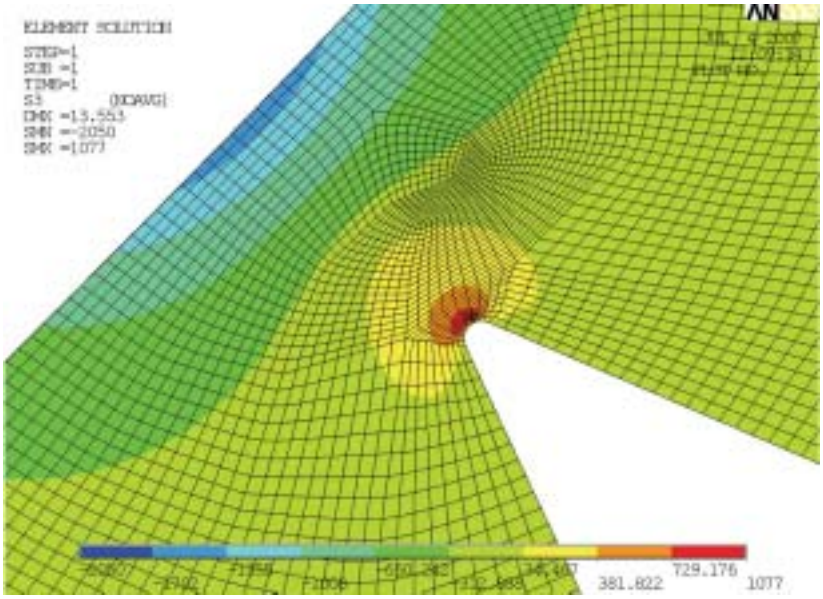


Figure 4:
Simulation of stress distribution for a notched silicon beam.

material degradation, crack propagation or fracture. For material parameter extraction finite element simulation (FEM) is used (see figure 4)

Nowadays reliability and robustness properties of MEMS devices are major performance factors. Apart from standardized test method MEMS specific accelerated test protocols are developed by Fraunhofer ISIT for assessing the reliability of MEMS. For lifetime operation, packaging, environmental impact and long term storage the failure mechanism and failure rates are currently under investigation.

Development of a Brushless-DC-Motor-IC as a Successful Start of the Partnership between TRINAMIC Motion Control GmbH & Co KG and Fraunhofer ISIT

Fraunhofer ISIT developed together with the company Trinamic a new IC for brushless DC motors (BLDC) including some new functionality. The project is funded by the Federal Ministry of Economic Affairs (BMWi) in the frame program Pro Inno II. With the first prototypes the main new features was tested successfully. The optimised chip will be introduced at the ELECTRONICA 2008 in November as a product to the customers.

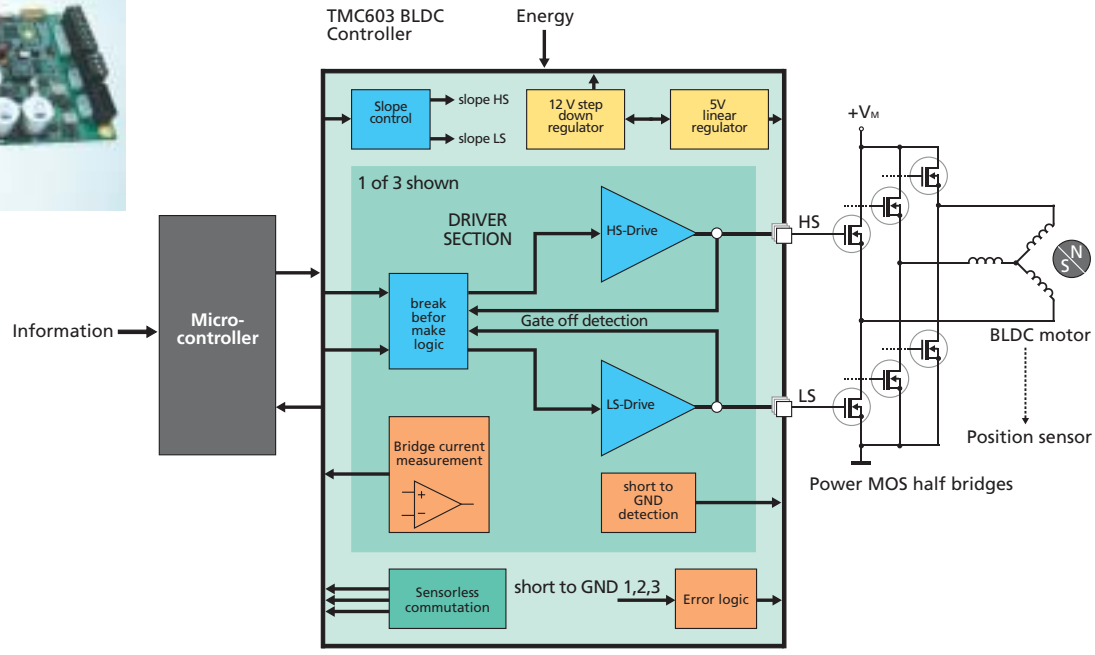
The BLDC motor features with a low-abrasive, even, and constant operation. An electronic circuitry takes over the commutation of the coils using a position sensor, that will be replaced in low cost applications by a sensor less measuring principle. There are BLDC motors in the power range from a few to several hundred watts. BLDC motors are used in all applications where long operating times and reliability are essential. Examples are computer devices or the industrial lab automation, e.g. in the medical technology.

In a prospective range the BLDC motors will remove the conventional, i.e. motors with brushes in more and more application fields.

The developed standard device TMC603 is optimised for the market of motors in the medium range power area. The device will steer the motor via an external MOSFET bridge that will be connected outside, see figure 2, and that has to be adapted to the motor power. The targeted applications always include a µ-controller, that takes over the control of the TMC603 and of the motor. The TMC603 therefore addresses all tasks the µ-controller can't offer, like the power part, current supply, and signal conditioning. The specific features of the device are the integrated measurement of the coil current, that don't need expensive shunt resistors, but uses the impedance of the MOSFET. The TMC603 in addition allows the commutation of the motors using an integrated Back-EMF measuring including signal conditioning. So any application can be changed

Figure 1:
Testboard with BLDC motor.

Figure 2:
Schematic of the new ASIC.



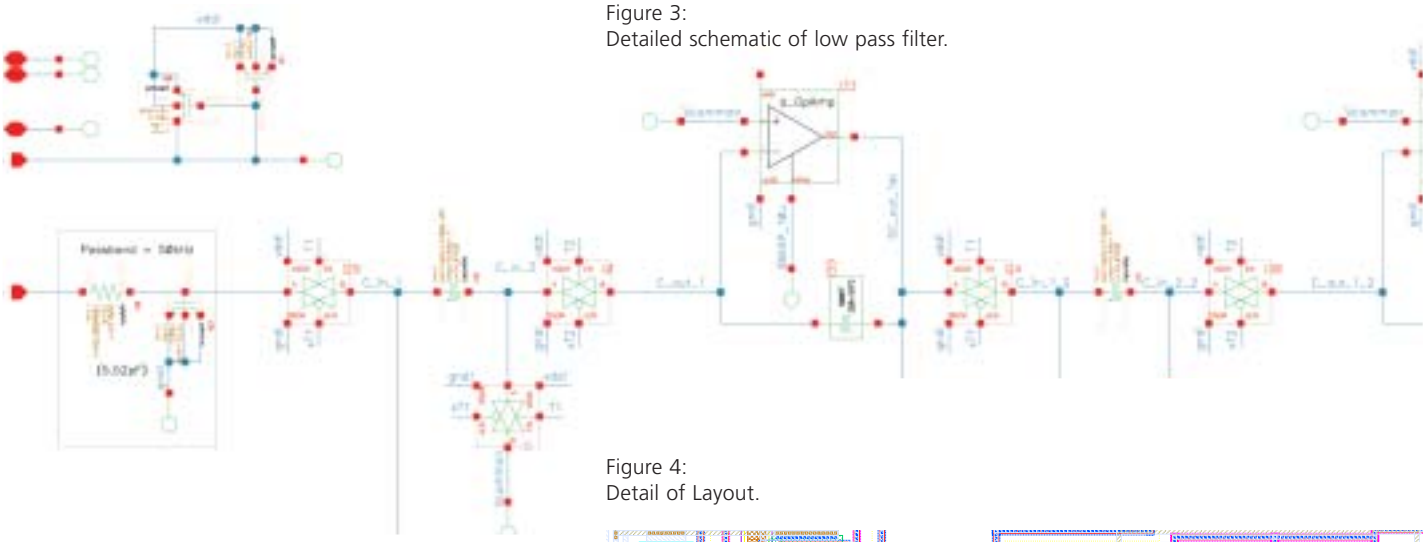
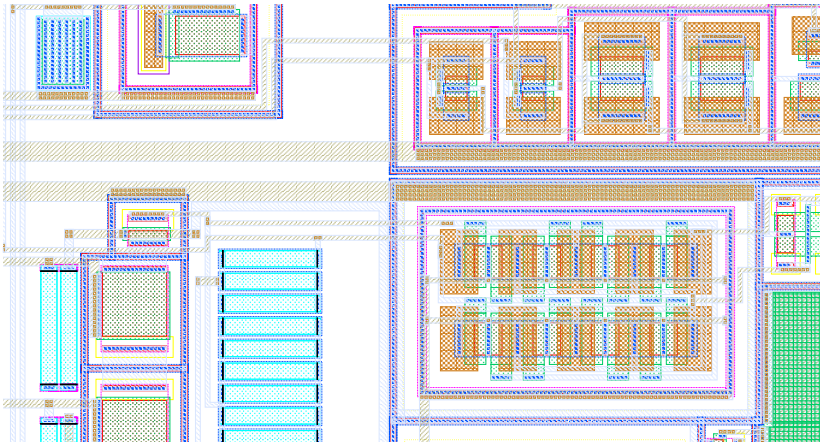


Figure 3:
Detailed schematic of low pass filter.

Figure 4:
Detail of Layout.



with few effort for programming and special hardware to a "sensor less" operation, i.e. the integrated hall sensors of the motor will not be used to measure the position. During the project a new method was developed that does not show the disadvantages of the known approaches and it was filed as a patent with the name "HallFX".

For the TMC603 device a modular 0.6 µm High-Voltage CMOS process is chosen, that offers several components for different voltage ranges. The design of such a smart-power-device, that allows to switch high currents at high voltage levels as well as to measure and amplificate sensitive analog signals in the mV range precisely, poses a high challenge in IC-Design including layout. At this point the application know how of TRINAMIC and the knowledge of ISIT supplemented very good. As an example the signal conditioning for the measurement of the current could only be realised to it's specification by using a chopper stabelised operational amplifier.

Outlook:
The TMC603 allows TRINAMIC the extension of the IC portfolio that was up to now focused to the BLDC-world. The device is the starting point for the development of a whole family of new devices, that shall be developed within the well proven cooperation of TRINAMIC and ISIT.

Figure 5:
Measured voltage of back commutation.

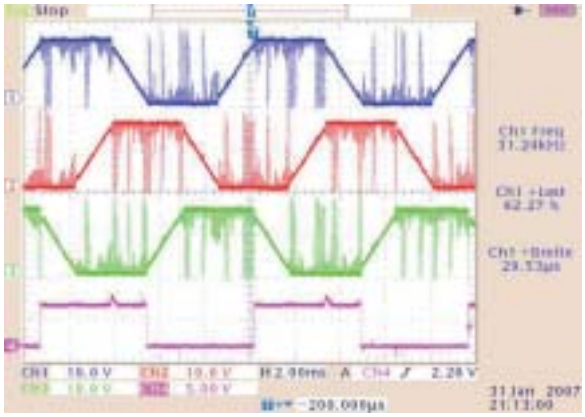
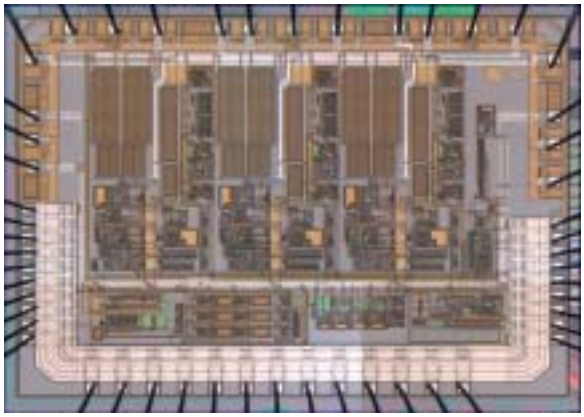


Figure 6:
View on the developed IC.

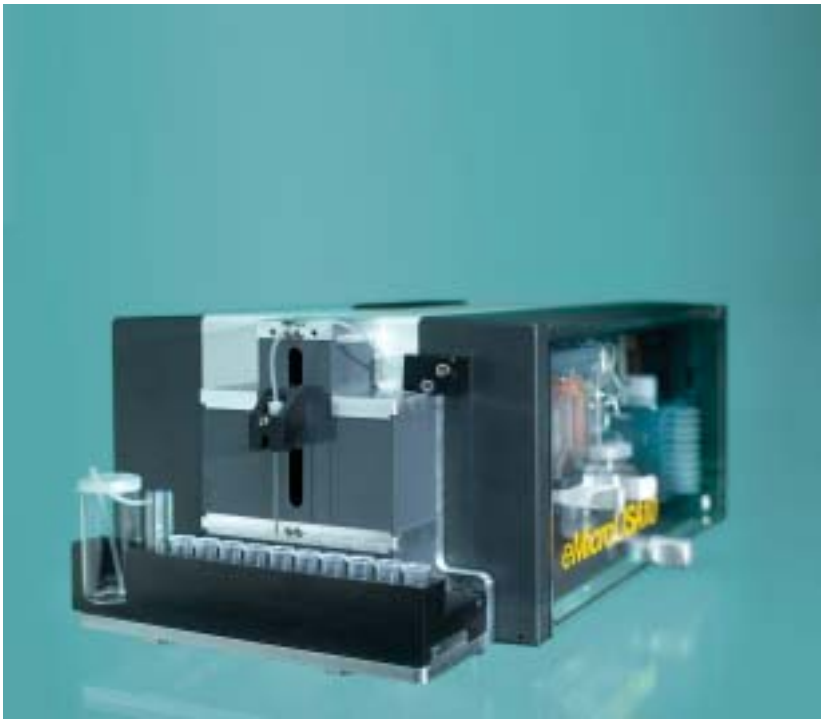


Advanced Automated Analysis System for Biowarfare Agent Detection

The department of biotechnological micro-systems (BTMS) of the Fraunhofer ISIT developed in cooperation with the company AJ eBiochip GmbH a measuring system for the readout of electrical biosensor arrays. These biosensors are suitable for a wide range of applications in areas as diverse as biodefense, biotechnology, medical diagnostics, and environmental analysis.
The types of substances which can be detected are DNA, RNA, proteins and haptens.

A key advantage of the existing analysis instruments "ePaTOX" and "eMicroLISA" are their automatic execution of assays after the reagents, sample and sensor chip are put in place.

Figure 1:
Sample-Changer.



This advantage will be further strengthened in a new device version by the addition of extra modules for automating sequential sample and chip exchanges for multiple assays. With this feature, the user avoids manual exchange of the chip and sample, thus greatly improving the working efficiency of the system. As part of a master thesis research, such a prototype device was developed which allows faster, sequential, and convenient execution of several analyses with minimal operator involvement. Furthermore, the new device uses optimized chipsticks.
A chipstick is a chip carrier with integrated flow channels that serves as a disposable item for convenient and safe handling.

At the moment each sample is manually inserted. In contrast to that the sample changer module can be equipped with several samples (see figure 1). The new chip exchanger is equipped with the appropriate number of disposible chipsticks.
A complete automation is realized by the synchronization of all the mechanisms involved in sample, reagent and chip supply. The withdrawal of the selected sample takes place via a steel capillary which can be moved up and down into each sample tube. It is decontaminated after each analysis in a separate rinsing container. This procedure is especially important in applications where decontamination is essential for the safe use of the devices, e.g., the detection of biowarfare agents or harmful pathogens. Every Chipstick from the magazine is automatically drawn in and contacted electrically, fluidically and thermally (see figure 2). Thereafter the sample and further assay specific reagents are carried over the electrical sensor chip by the automated fluidic system. A successful miniaturization of the new modules is confirmed by the integration into the existing housing of the analysis instrument.

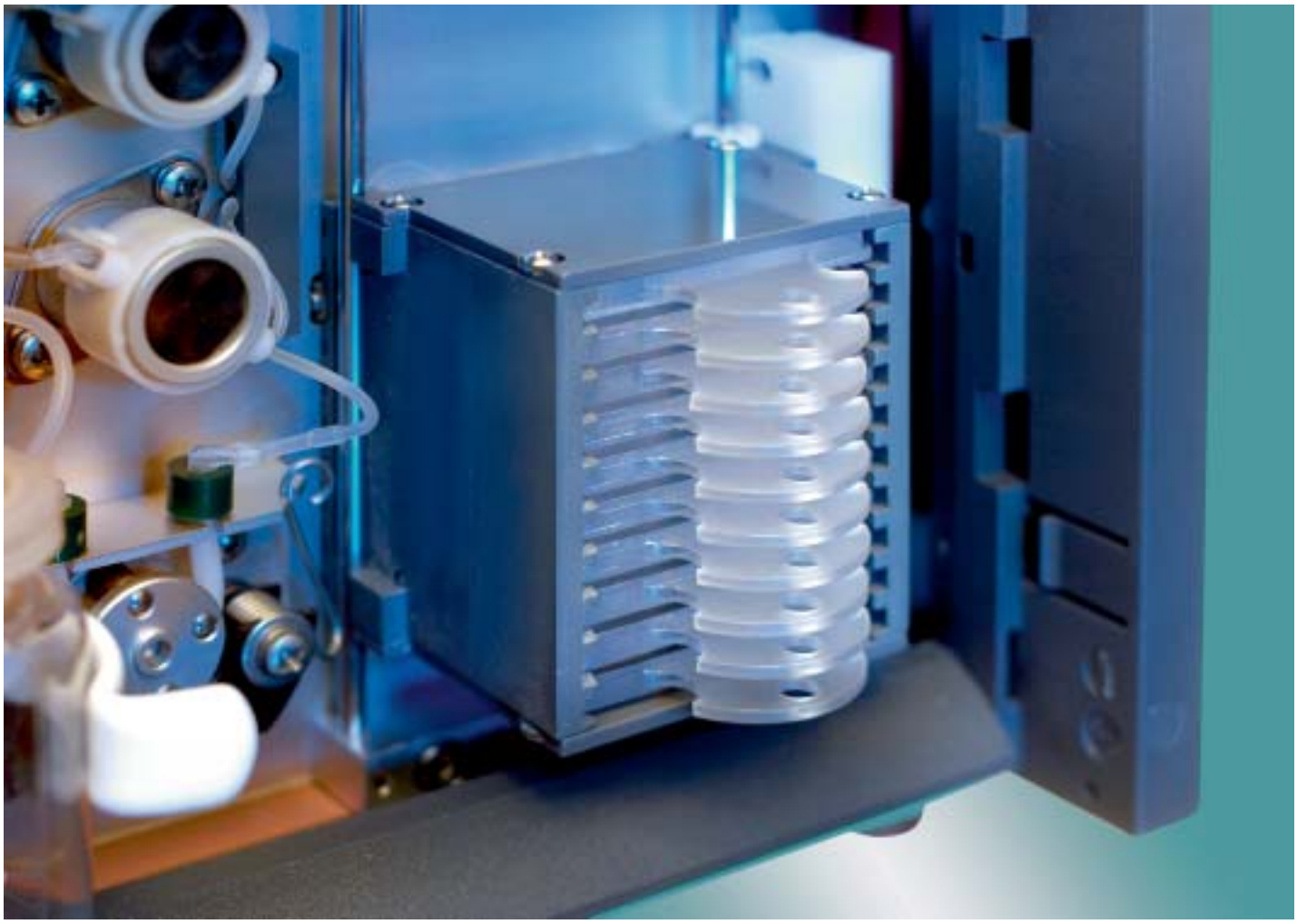
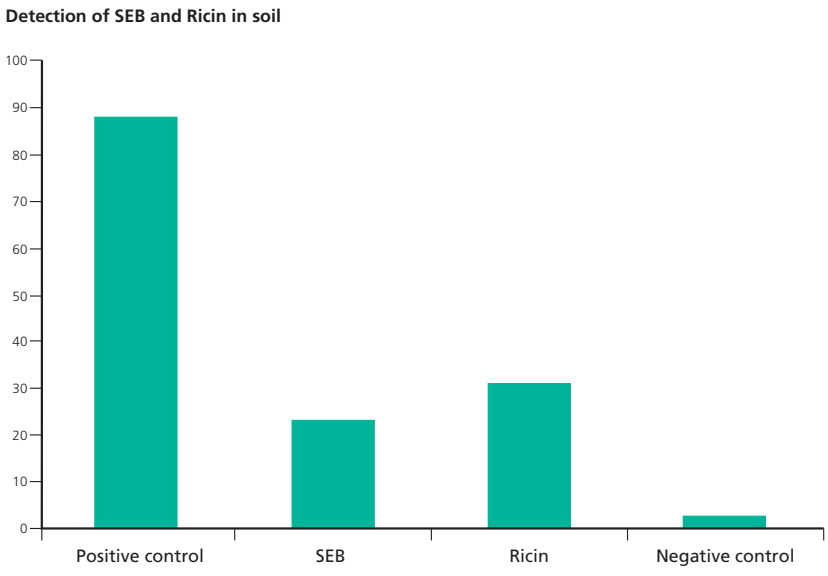


Figure 2:
Chip-Exchanger.

Figure 3:
Measurement result for the detection of spiked soil. 100 mg of soil were spiked each with 5 ng SEB and Ricin. Before measurement, the soil was suspended in buffer solution (1 ml) and filtered. The measurement was carried out on a 16 position array chip using an ePaTOX device.

Future applications and the first tests will focus on the detection of biowarfare agents. In this field, special care is required for the handling of probes and detection systems in order to protect the users from possible dangers caused by biological toxins and microbial pathogens. At Fraunhofer ISIT and AJ eBiochip, the detection of several biowarfare toxins and pathogens on electrical biochips was successfully developed. An example for the measurement of a real probe is presented (see figure 3): It shows the detection of spiked soil with the bacterial toxin Staphylococcus enterotoxin B (SEB) and the plant toxin Ricin from Ricinus communis.



Representative Results of Work Module Integration

Solutions for Image Sensor Packaging

Compact camera modules are widely used in mobile phones. Further cost reduction potential and quality enhancement is expected from wafer level packaging approaches by stacking lenses and the imager chip to form tiny camera cubes with resolutions up to 5 Megapixels in only a few process steps.

Today, new market potentials are opened in industrial automation and car driver assistance systems. They require robust systems with the capability to pre-process the sensor output for optimized contrast and brightness in a large variety of light situations. Fixed-pattern noise correction suppresses artefacts to improve machine vision reliability, which is a basic requirement for safety-related applications that use automatic object recognition.

Real-time image processing requires high calculation efforts - yet, a full computer core with processor and memory chips, power supply and bus transceivers generates a high amount of heat. For a thumb-sized smart camera, this means that the image quality will suffer if no efficient thermal control can be realized.

Imager packaging and thermal analysis for an automotive vision system were two of Fraunhofer ISIT's tasks in the German project µCAM. To reduce the costs of image sensor mounting, hybrid technology (soldering and wire bonding) shall be replaced by surface mount technology. ISIT investigates in two packaging approaches to reduce the overall system costs:

Figure 1:
Through-Silicon Vias (TSV) in thick wafers are targeted for chip-scale packaging of image sensors. The figure shows a sample cross-section with metallized vias in a test chip.

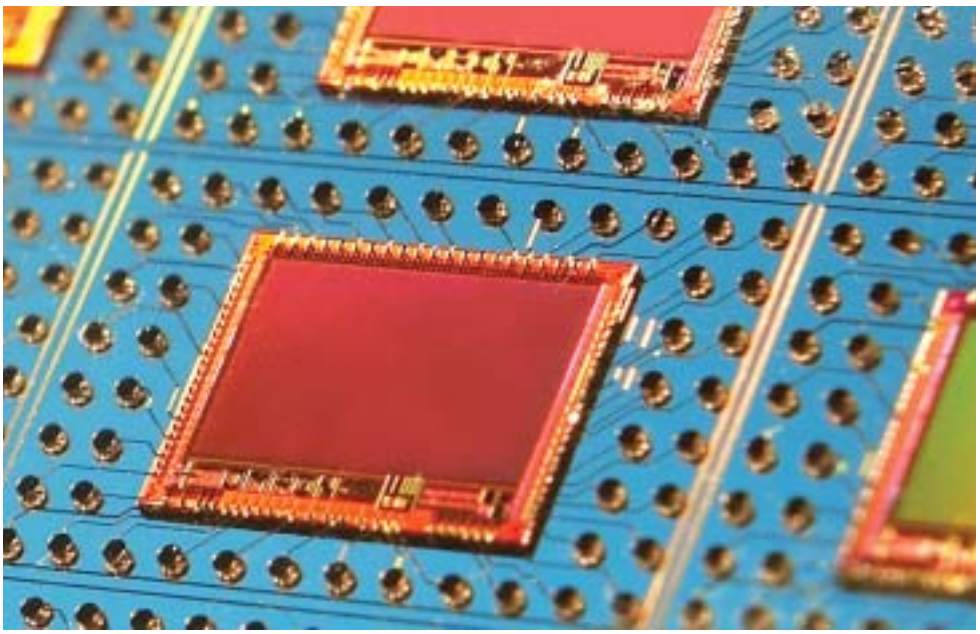


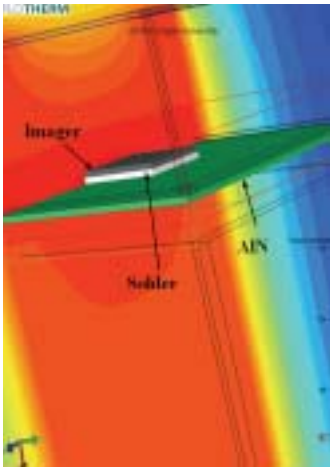
Figure 2:
A glass chip is used to spread the contact pads of the image sensor to a surrounding solder ball array. Using flip-chip-technology, antireflection coating and solder balling, a surface-mount device is formed from the image sensor. Underfilling can enhance the reliability of the assembly.

Chip-Scale Imager Package

With post-CMOS via technology, the frontside contacts of the image sensor chip are redistributed to the backside. An array of 48 solder balls on the 6 x 8 mm² area allows conventional SMT placement, lifetime reliability can be improved by an adhesive underfill. This approach is equally suitable for chip stacking on an ASIC, if an adequate contact array can be realized in the design.

Imager Contact Redistribution by Flipchip-on-Glass technology

As an alternative approach, the imager can be placed face down on a glass carrier chip. Although the contact redistribution to a peripheral solder ball array around the chip will enlarge its area to 10 x 12 mm², enhanced protection of the sensor surface against scratches is given. With anti-reflection layers, sensitivity loss can be minimized in a selected spectral range. Further packaging steps like underfill are equally recommended for a long-term reliable board connection.



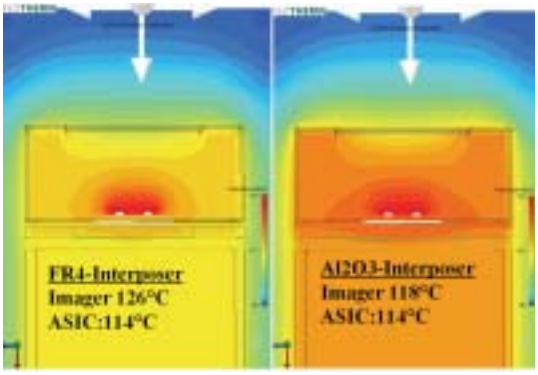
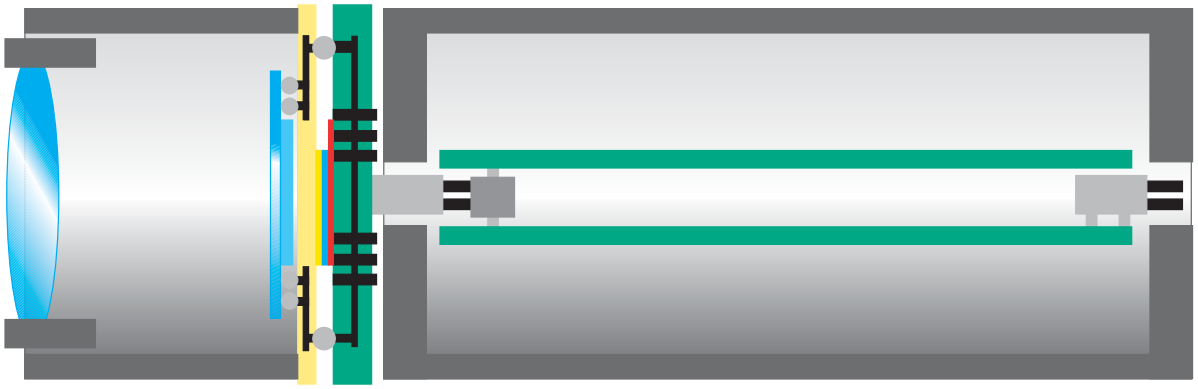


Figure 3:
With 95°C ambient air temperature and max. 120°C for the imager, cooling becomes critical. Imager and ASIC are mounted on a ceramic heat-spreader. The thermal simulation shows that a good lateral distribution can be achieved if a good thermal contact between chip and substrate is given.

Figure 1:
Concept study for a microcamera prototype integration (approx. 70x 20x 20 mm³). The camera head integrates an image sensor (here: flip-chip on glass carrier for contact redistribution), an ASIC chip and the lens optics. The right-hand box contains the core module with high power dissipation (3,5 W).



Representative Results of Work Module Integration

Analysis of Solder Heat Resistance of Surface Mount Devices (SMD) and Printed Circuit Board (PCB) Substrates

Due to higher solder temperatures (up to 260°C) using lead free Tin Silver Copper (SAC) solder alloys the question of solder heat resistance is more up to date than ever. The thermal load during solder reflow could cause damage of PCB material and plastic encapsulated Surface Mount Devices (SMDs) which are sensitive to moisture-induced stress.

When epoxy materials are exposed to the high temperature of solder reflow the vapour pressure of moisture inside the epoxy materials increases greatly. Increasing the solder peak temperature from 225°C up to 260°C the vapour pressure of moisture raises from about 25 bar up to 47 bar. This can generate e.g. delamination, bond lifting, die lifting or internal and external package cracks. The Moisture Sensitivity Level (MSL) indicates the susceptibility of nonhermetic solid state SMDs due to absorbed moisture during reflow soldering process. Components with MSL 3 are allowed to be exposed environmental conditions of at most 30° C/60 % RH for at most 168 h before they are reflowed. Such components which are used for a lead contained reflow soldering process have to be classified for the higher reflow temperatures of a SAC soldering process. To identify the classification level of nonhermetic solid state SMDs a test procedure is recommended in IPC/JEDEC J-STD-020D.

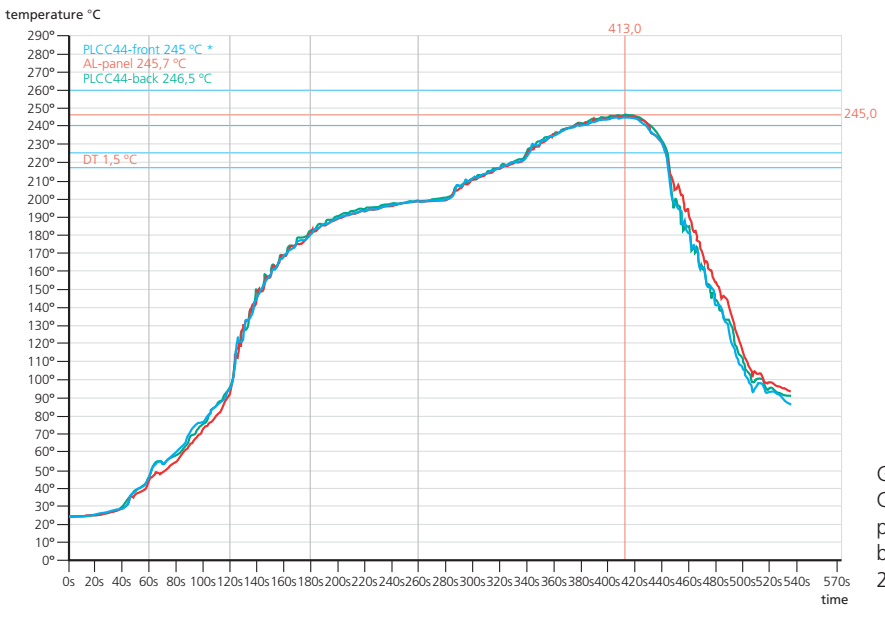
A defined amount of sample units has to pass through the following process steps:

- Initial Electrical Test
- Initial External Visual Inspection
- Initial Acoustic Microscopy
- Bake
- Moisture Soak
- Reflow
- Final External Visual Inspection
- Final Electrical Test
- Final Acoustic Microscopy

Graph 1 shows a typical classification convection reflow profile for Pb-free Assembly with a classification peak package body temperature of 245°C. If one or more devices in the test sample fail, the package shall be considered to have failed the tested level. A device is considered a failure if it exhibits one of the following criteria:

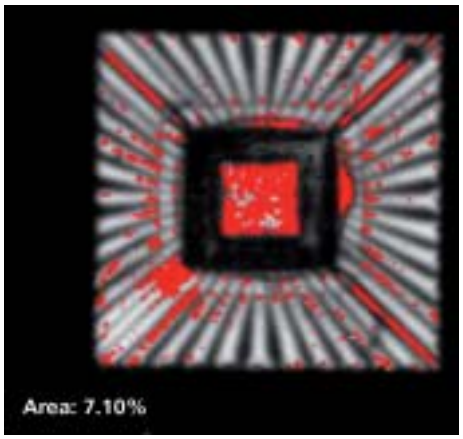
- External crack visible
- Electrical test failure
- Internal crack
- Changes in package body flatness which are out of co-planarity and stand off dimensions

With an acoustic microscope which creates an image using ultrasound to view a specimen's surface or subsurface features, components are analysed non-destructive. Figure 1 shows an acoustic microscopy inspection of a PLCC44



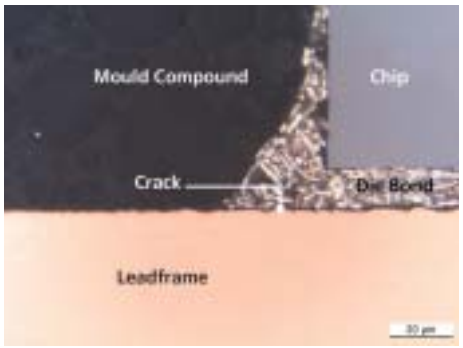
Graph 1:
Classification reflow profile, peak package body temperature 245° C.

Figure 1:
Acoustic microscopy of PLCC44 after reflow load.



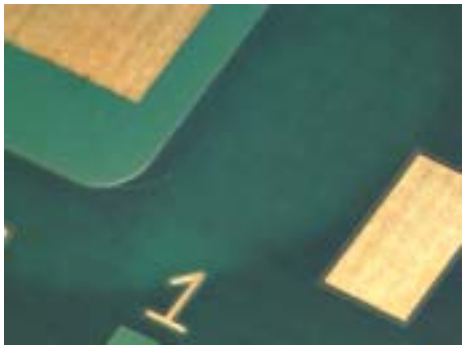
component after the reflow load. Red areas show delamination within the mould compound of package and within the die bond of the chip. If internal cracks are indicated by acoustic microscopy they must be considered a failure or verified good using microsection through the identified site. The corresponding microsection, which is a destructive analysis method, is shown in figure 2. A separation between the leadframe and the die bond is visible.

Figure 2:
Microsection of PLCC44 after reflow load, crack visible.



Due to several high temperature soldering processes PCB substrates are exposed to several thermal loads. The typical electronic assembly has to pass through during its production at least two reflow cycles and one selective soldering process. If there is a defective component like a BGA or QFN on the assembly two more reflow cycles are necessary to change this component.

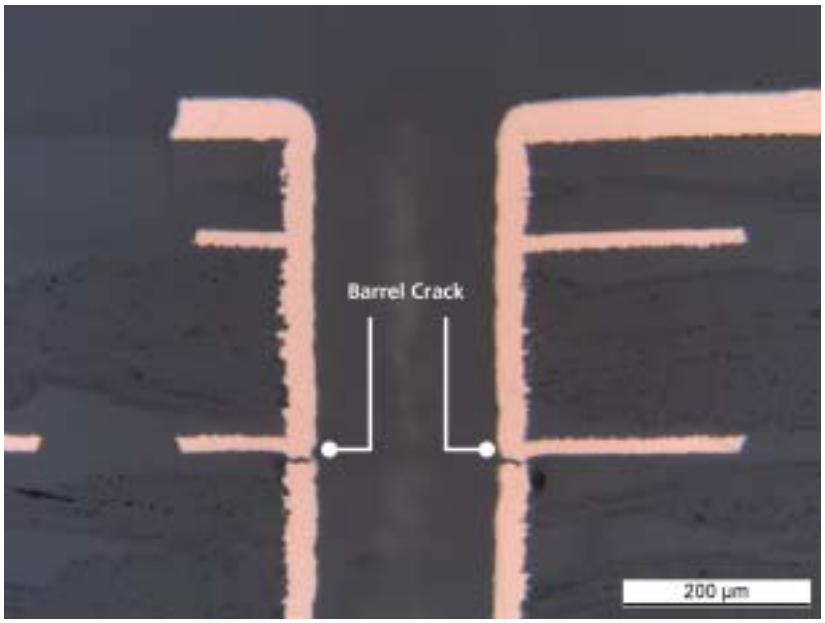
Figure 3:
Delamination of PCB substrate after 4 times reflow simulation, 260° C



To verify if the substrates withstand this accumulated thermal stress they are exposed 3 – 6 times to a convection reflow process with a maximum substrate temperature of 260° C. An optical inspection is performed to identify delamination or other optical changes of the substrate material. Figure 3 shows a PCB substrate with delaminated areas after 4 times reflow simulation.
Electrical tests are performed to verify electrical parameters, like value of resistance.

The substrate integrity is analysed by microsection. Specially Plated Through Holes (PTH) tend to perform internal cracks by excessive z-axis expansion of the laminate material during the reflow process, see figure 4. Due to a higher z-axis Coefficient of Thermal Expansion (CTE) than the plating copper the epoxy resin expands more in z-direction. This results in partial damage like innerlayer separation up to plating cracks in the corner or in the barrel of the PTH.

Figure 4:
PTH crack after reflow simulation, 4 times 260° C.



Verification of solder heat resistance of SMD and substrates are performed at the ISIT LEADFREE Training Line. Components and PCB materials can be qualified for customer defined reflow profiles and demands.

Current Tin Whisker Know How

Background and Definition

Lead-free solder joints require first of all suitable solder alloy compositions, which typically means changing towards tin-rich solders. In Europe, lead-free PCB (Printed Circuit Board) assembly solder is generally based on Sn-Ag-Cu alloys with melting temperature ca. 40°C higher than that of eutectic tin–lead alloys. Therefore, the materials used for assembly must withstand higher solder process temperatures in the lead-free production. Furthermore, solderable finishes on sub-strate (solder pads) as well as on component terminations (leads) must be composed of materials avoiding banned sub-stances.
As tin is the major constituent of almost all alloys for soft soldering, pure tin as a solderable finish is a straight-forward choice; however, pure tin layers were found prone to whisker growth already in the 1950s, whiskers leading to electrical shorts (figure 1).

Tin whiskers are needle shaped single crystals growing out of plated tin surface layers, due to internal compressive stress acting in the layer. Formation and growth can can take place within hours, days or weeks. JEDEC 22a121-01 defines a method to measure tin whisker length, and characterises whiskers by an aspect ratio (length/diameter) of larger than 2. Whiskers can be straight, kinked, bent or twisted, and have a uniform cross section. Usually a whisker is a standalone column shaped structure, seldomly branched. Horizontal stripes or rings around the base are possible, indicating a periodic growth during temperature cycles (figure 2 a-d).
Tin whiskers can grow to a length of several mm while only one to a few µm in diameter.

Figure 1:
An early tin whisker growth experiment at Bell Laboratories in 1953. Tin whiskers growing on a tin plated steel specimen. Note short circuit failure potential of the long conductive tin whiskers. From Ellis, Gibbons und Treuting, Bell Telephone Laboratories, Murray Hill, New Jersey. Source: The American Competitiveness Institute http://www.aciusa.org

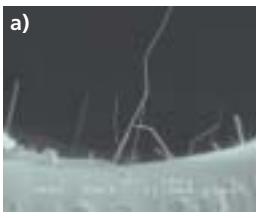
Problems

Tin whiskers grow from PCB pads as well as from component leads and terminations. Especially fine pitch applications are endangered by whisker shorts (figure 3). They can penetrate 25 µm of conformal coating (figure 4). Whiskers will lead to signal defects, but can also carry rather high currents in the order of 30 to 75 mA before fusing. The tables "whisker risk factors" lists essential problems whiskers can cause in microelectronics and microsystems products.

Longterm-Behaviour

In 1987, B. D. Dunn presented ESA publications showing high quality SEM images from tin whiskers to strongly discourage from the use of pure tin, zink, and cadmium platings for space applications (figures. 2, 3). Instead, eutectic tin-lead finishes were recommended as a viable alternative minimizing tin whisker risk (see the webpage http://esmat.esa.int under Publications).
In a recent remarkable publication (TEC-QM/06-388/BD/MH) Dunn showed results, having revisited his earlier samples after 15 years at room temperature. After all this time, no tin whiskers were found on fused tin platings on brass, copper-plated brass, and steel.
With electroplated tin, whiskers grew to a length of 1 to 3.5 mm on brass, copper plated brass, and copper plated steel. On steel without copper plating, whisker growth stopped after two years at a length of 10 to 20 µm. In all cases, nucleation periods from one to six months were

Figure 2:
a) Immersion tin plating on a through hole via in PCB (ISIT).
b) Whiskers growing from a component surface layer (source: JEDEC).



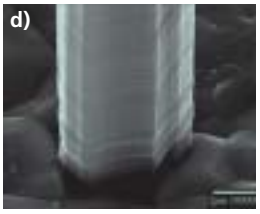


Figure 2:
c) „Hillock" on a surface; not (yet?) a whisker (Dunn).
d) typical column with edges; cross striation growth shapes form in temperature cycles (JEDEC).

Damage mechanism	Description
Stable Short Circuits in Low Voltage, High Impedance Circuits	a tin whisker can carry more than 50 mA before fusing open
Transient Short Circuits	experienced as the whisker fuses open at atmospheric pressure
Metal Vapor Arcing (plasma) in Vacuum	With sufficient current and above 12 V supply voltage, vaporized tin may initiate plasma that can conduct over 200 A
Debris/ Contamination	may bridge isolated conductors; whisker debris may interfere with optical surfaces or MEMS structures

Table 1:
Tin whisker risk factors (Pinsky, Osterman, Ganesan 2004).

observed before notable whisker growth started. Contaminated tin plating was worse than the other.

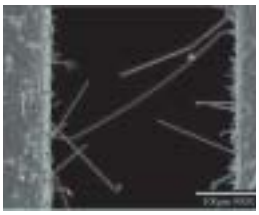
Formation of Tin Whiskers

Whisker formation is attributed to internal compressive stress from early theoretical contemplation. Under pressure from the side, the material grows out of plane, this way avoiding stress. There are five ways for the evolution of compressive stress in leadframe finishes:

- Internal stress due to inclusions/contaminations in tin, e.g. organic plating bath constituents, which are implanted in the layer during the wet chemistry process; this can be avoided by proper choice of chemistry and process control
- Bending of a finished leadframe ("trim and form"process)
- By accidental scratches or dents in the surface
- By temperature cycles of joined materials with difference in the coefficient of thermal expansion; here especially true for Sn-layers on Fe-Ni leadframe ("Alloy 42")
- By inhomogeneous growth of Sn-Cu intermetallic phase particles in the interface; this goes for Sn layers on copper leadframes without nickel or other barrier layers.

Examples of intermetallic growth along tin-base metal interfaces are shown in figures 5a-c. Copper base metal reacts far heavier with the tin layer than nickel-tin or tin silver, see SEM images of tin on iron-nickelbase metal (e. g. alloy 42).

Figure 3:
Needles and electrical short over ca. 280 µm spacing (Dunn).



Test Acceleration and Reliability

JEDEC 22a121-01 provides a number of tests to standardise an industry accepted method for measurement, a com-parison of the tin whisker growth propensity of various plating and metallisation chemistry and process; and a con-sistent inspection protocol and reporting standard for whisker investigations. This standard also refers to the study "Recommendations on Lead-Free Finishes for Components Used in High-Reliability Products", published by the iNEMI Tin Whisker User Group in July 2005. This study can be viewed on the iNEMI internet pages.

Meanwhile, viable industry guidelines and standards were published for whisker quantification, testing, and mitigation practice, as there are the JEDEC document JESD201 "Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes". This acceptance standard is based on JESD22A121.01 "Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes"; measures against whisker growth are described in JP002 "Current Tin Whiskers Theory and Mitigation Practices Guideline". In February 2007, ZVEI published a pamphlet titled "Pb-frei": Whiskerarme Sn-Oberflächen, Verarbeitbarkeit, Löten und Lötwärmebeständigkeit für Automotive Anwendungen" (Pb-free: Low-whisker Sn surfaces, processability, soldering, and solder heat resistance for automotive applications); this pam-

Figure 4:
a) "Tent formation" in acrylic resin conformal coating of 100 µm layer thickness (278 days at room temperature + 137 days at 50°C/50%RH) (Woodrow).
b) Whisker penetrating silicone conformal coating (layer thickness 22 µm, 278 days at room temperature + 419 days at 50°C/50%RH) (Woodrow).

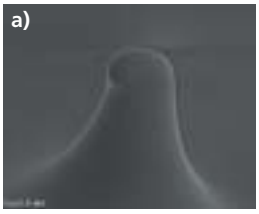
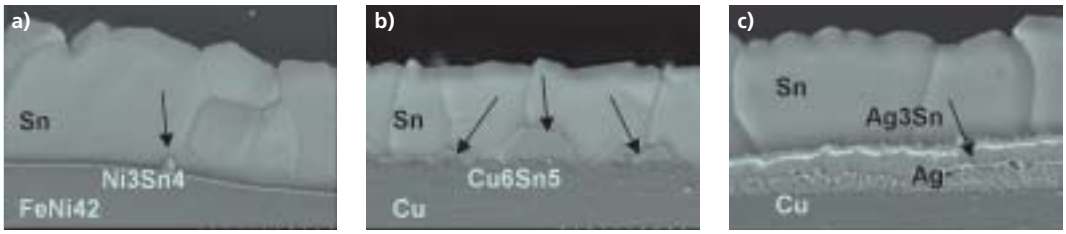


Figure 5:
a) Pure tin on alloy 42.
b) Pure tin on copper.
c) Pure tin on silver.



phlet refers to the international Standard IEC60068-2-82 "Environmental testing - Part 2-82: Tests - Test Tx: Whisker test methods for electronic and electric components".

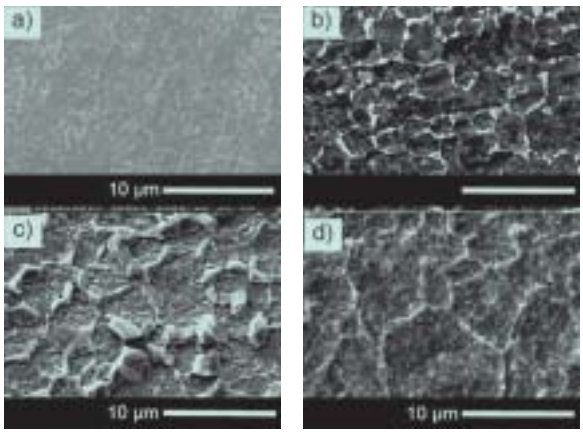
The dilemma of whisker test or verification, let alone reliability testing is that whisker growth mechanisms appear to be very sensitive to temperature. The mechanisms themselves depend on the combination of layer and base material, and there is a noteable influence from plating contaminations. Taking copper-tin phase growth as example, here the compressive force leading to whisker growth is formed by inhomogeneous phase particle formation at room temperature. At a temperature of 150°C, the intermetallic copper-tin phase forms a homogeneous layer leading to stress relaxation, this temperature level is even used for a whisker mitigation treatment. So temperature increase as thermal activation may only be very moderate; industry standards propose +55°C. Temperature cycles to accelerate tin plating on copper may also not exceed the range from -55°C to +85°C; for tin on steel, the upper range may be up to +125°C. "Storage (+30°C/60%rel.H.)" and "high temperature / humidity (+55°C / 85%rel. H)" conditions are also moderate. Due to noteable nucleation times and slow growth, test times of 2000 to 4000 h are necessary for process verification or material qualification. True reliability testing would take years, and still problems can be encountered by mechanical handling such as bending and scratching. This needs to be ac-counted for when components are applied in a critical product, where mechanical processing is part of the manufacturing flow. Examples are press fit connections made during the manufacturing or mounting of connectors.

Mitigation

In accord with current standards, whiskers are considered uncritical for fine pitch applications when their length does not exceed 40-45 µm (JEDEC JESD201) resp. 50 µm (IEC 60068-2-82) after testing, as agreed between supplier/ manufacturer and customer.

Various practices developed and recommended against tin whiskers over the past few years are shown in the table 2. Established procedures are the "post bake" for leadframe based solid state devices (figure 6), and plating followed by mechanical treatment for small passive components (figure 7). In addition, conformal coatings can reduce whisker growth somehow. Normal thickness CC (25 µm) will be penetrated by whiskers, but thick coatings from 100 – 150 µm keep whiskers enclosed and appear to be the

Figure 6:
Showing Cu-Sn-phase layer growth by selective etch removal of tin layer, reasoning tin whisker mitigation strat-egy for semiconductor leadframe packages by Post Bake of 1h at 150°C within 24 h following electrochemical tin plating on copper (from Dittes, Oberndorff, Petit, Crema; Tin Whisker Investigations and Countermeasures).
a) 1 h after deposition. b) 6 d after deposition.
c) 7 w after deposition. d) 1 h 150°C directly after deposition.



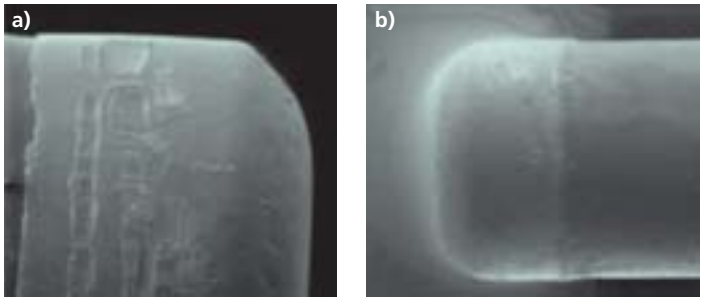


Figure 7:
a) MELF resistor terminal after 15 years of storage, not soldered, pure tin finish; no whisker formation, not even on surface scratches.
b) Pure tin terminal, mounted on PCB (SnPb soldered), after 6 years in service in automotive application; no whisker formation visible.

only proper means for assembly manufacturers to actively reduce whisker risks. Parylene layers show the best, acrylic layers the least effect, these will be lifted or penetrated by whiskers, as will be silicone layers (see figures 4 a and b).

Table 2:
Tin whisker mitigation measures.

Recommendations	Control factors
Use of matte tin	Organic additives („brightener") used to promote surface brilliance increase the propensity for whisker formation by compressive stress acting from the inclusions into the surrounding metal crystal. Matte tin contains less organic inclusions and is therefore found non critical by many component manufacturers, but not by all end users.
Reduction of organic contaminations	Beside the decision for matte tin, further organic impurities in galvanic plating baths have to be controlled, which otherwise might be implanted leading to compressive stress.
Plating thickness < 0.5 µm Plating thickness > 10 µm	A tin plating thickness less than 0.5 µm, or more than 10 µm is recommended to gain reduction in whisker formation risk as compared to intermediate plating thickness
„post bake" heat treatment 1h at 150°C	A treatment of 1 h at 150°C within 24 h of plating yields an increased but even thickness copper-tin intermetallic phase layer. This prevents later formation of inhomogeneous copper-tin phase particles, which could as single chunky imperfections in grain junctions impose compressive stress on neighbouring grains. Not all end users accept this heat treatment to components. The E4 group (Philips Semiconductor, Infineon, ST Microelectronics und freescale), however, recommends this "post bake" after extensive mitigation verification tests.
Fused tin plating	Reflow at temperatures above pure tin melting point changes the plating layer microstructure favourably by grain growth and relaxation of internal stress. Thus, driving force for whisker growth is reduced.
Melt tinning	Large grains and favourable even thickness copper-tin intermetallic phase layer yields negligible propensity for whisker growth.
Ni-Barrier > = 2 µm	An effective nickel diffusion barrier on discrete passive components has a thickness of minimum 2 µm between tin and base metal.
Alloy content > 2%	A notable effect of alloy constituents on tin whisker mitigation needs minimum 2% alloying element. 10% to 20% was used in the case of lead. However, since lead is banned by environmental legislation, some Japanese semiconductor manufacturers use 2% bismuth, being compatible with the use of tin-silver-bismuth solder alloys used in reflow solder paste by Japanese assembly houses; 2% bismuth is also viewed non critical in mixtures with tin and lead. However, certain high reliability users do not permit the use of bismuth in tin plating.
Cu leadframe	Nickel-iron leadframes („Alloy 42" = Fe-42wt.%Ni) build up deformation strains in temperature cycles. These strains may yield whisker formation. Reason is the low coefficient of thermal expansion of alloy 42 in comparison to tin (CTE of alloy 42 = ca. 3 ppm/K, CTE von Sn = 22ppm/K). In this account, copper is a better match for tin (CTE of Cu = 17 ppm/K).
Alternative end finishes • Ni-Au • Ni-Pd • Ni-Pd-Au	Naturally, any surfaces free of tin will not form tin whiskers. One useful example is the so called „pre plated" finish, plated on the leadframe base metal for die attach and wire bonding. With these finishes however, solderability may become more of an issue than with matte tin. Examples of these high melting metal finishes see left.

Representative Results of Work
Integrated Power Systems

ISIT Battery Technology for Automotive Industry

The success of the Toyota Prius hybrid electric vehicle, the ongoing discussion on reduction of CO_2-emission from cars and the increasing need to reduce fuel consumption due to rising oil prices have strong impact on the German automotive industry. Hybrid electric vehicles (HEV's) or as a long term option electric vehicles (EV's) are currently becoming subject of major development activities of German car manufacturers. A key component is the electrical energy storage device. Lithium-ion based secondary batteries are, besides fuel cells, the most promising technology for these applications especially due to their high energy density.
Such cells have up to now been optimized for use in consumer applications. But in automotive applications the battery faces much more challenging requirements: safety, high energy and high power density, long-life cycle, broad temperature range at low costs are the most important ones (see figure 2). The properties of cells can be modified by introduction of new materials for the electrodes as well as for the electrolyte and by an appropriate design of cells.

Fraunhofer ISIT has developed in the past decade a stable process for manufacturing of Lithium-polymer secondary batteries. Based on this process ISIT is currently optimizing and testing new cell chemistries for their use in HEV- and/or EV-storage devices. Special focus is put on systems utilizing Lithiumtitanate ($Li_4Ti_5O_{12}$) as anode material. This material is characterized by its excellent cycle-life and shelf-life properties as well as its superior inherent safety features in combination with different cathode materials and by this addressing some of the key issues of batteries for automotive application.
Two examples from cycling of Lithiumtitanate-based system are shown in figure 3.

Titanate-based systems may be combined either with conventional electrolytes for standard Lithium-ion cells or with new electrolytes to e.g. extend the temperature range of operation or to further improve safety e.g. with respect to flammability and/or gas formation in the cells. High current capability (charging and discharging) in such cells can be achieved by using fine sized or even nanocrystallinic Lithiumtitanate particles in the anode. One challenge left is the improvement of energy density in this system. Projects addressing this aspect are on the way.

Cells with capacities up to 40 Ah have already successfully been built and tested. Table 1

Figure 1:
Prototype of high performance Lithium rechargeable battery for automotiv applications.

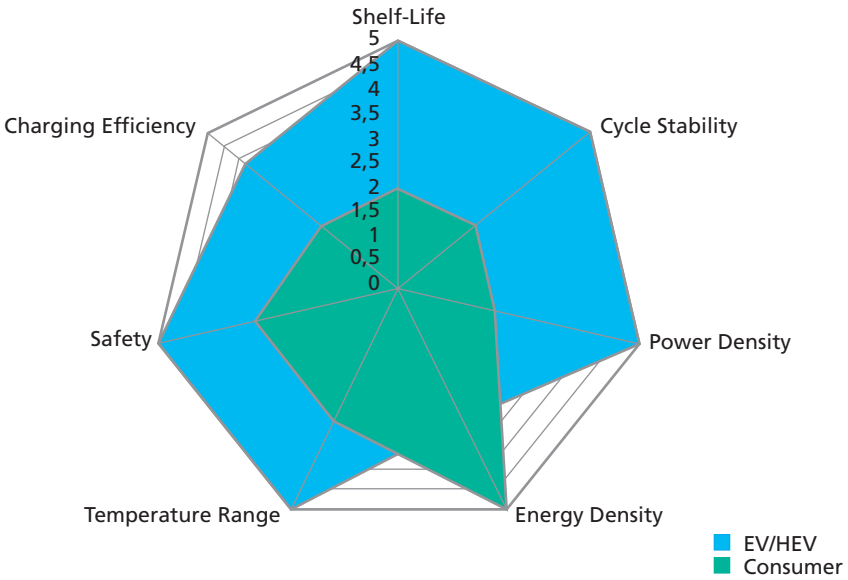
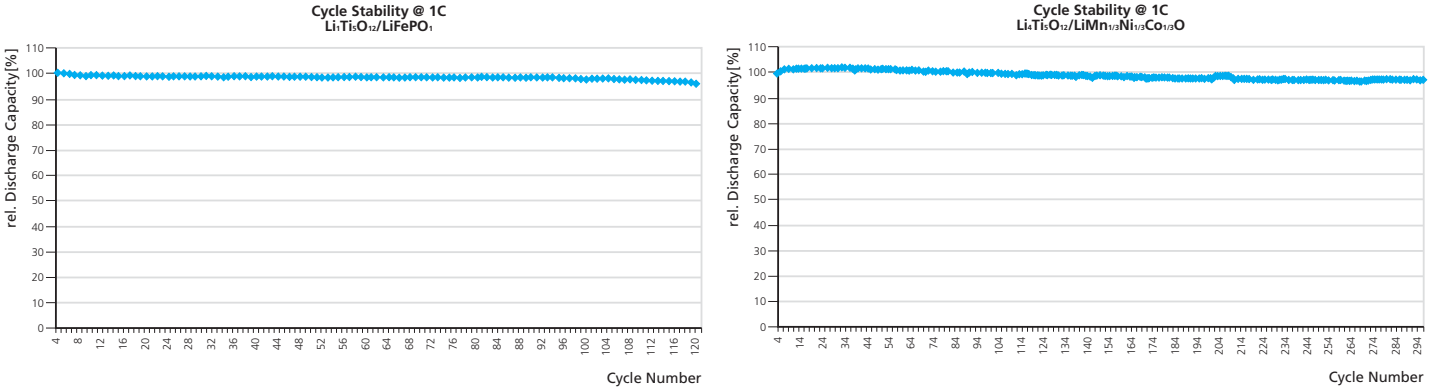


Figure 2, above:
The most important factors that secondary batteries in automotive applications have to face in comparison to consumer cell properties.

compares the main features of common consumer cells to new cells containing Lithiumtitanate as anode material.

Besides optimizing of cell chemistry and set-up the system integration and battery management is another big issue because up to hundred or more cells have to be switched in series to achieve the favourable voltage level of some 200 V to 400 V typically used in cars. Power electronics and a complex battery management system including hardware and software are needed as well as a powerful cooling during operation. Together with other Fraunhofer Institutes ISIT is involved in the development of such battery management systems.



Technical Feature	Graphite	Lithiumtitanate	Remarks
Energy Density	high	limited	
Nominal Voltage	3.6 V ... 3.8 V	1.8 V ... 2.4 V	depending on cathode material
Cycle-Life	limited*	Very high (> 5000)	* depending on depth of discharge
Shelf-Life	limited	Very high	
Self discharge rate	low*	Very low	* Depending on storage conditions
Inherent safety	critical	high	
Temperature range	limited	wide	Electrode particle size, electrolyte
Deep discharge	critical	stable	
High current capability	low to high	low to high	depending on electrode particle size and cell layout

Figure 3, above:
Cycle stability of a cell with a $Li_4Ti_5O_{12}$-anode and a $LiMn_{1/3}Ni_{1/3}Co_{1/3}O_2$ or a $LiFePO_4$-cathode, respectively, with standard electrolyte LP30 at room temperature both showing an extraordinary low capacity fading.

Table1, left:
Comparison of key features in automotive application of Lithium-based rechargeable cells distinguished by the anode material selected.


Important Names, Data, Events
Annual Report 2007

Lecturing Assignments at Universities

H. Bernt:
Halbleitertechnologie I und II,
Technische Fakultät der Christian-Albrechts-Universität, Kiel

R. Dudde:
Honorary Professor, Mikrotechnologie, Fachbereich Technik, FH Westküste, Heide

A. Heuberger:
Lehrstuhl für Halbleitertechnologie, Christian-Albrechts-Universität, Kiel

O. Schwarzelbach:
Mikroelektromechanische Systeme (MEMS),
Institut für elektrische Messtechnik und Mess-Signalverarbeitung,
Technische Universtität Graz, Austria

B. Wagner:
Micro- and Nanosystem Technology I and II,
Technische Fakultät der Christian-Albrechts-Universität, Kiel

Memberships in Coordination Boards and Committees

T. Ahrens:
Member of AOI-Anwenderkreis (Automated Optical Inspection)

T. Ahrens:
Member of DVS Fachausschuss Löten

T. Ahrens:
Member of Hamburger Lötzirkel

T. Ahrens:
Chairman of DVS AG 63 „Ausbildung Weichlöten in der Elektronikfertigung"

J. Eichholz:
Member of MEMS and Sensor Systems, DATE ´08 Conference

J. Janes:
Member at MEMUNITY, The MEMS Test Community

K. Pape:
Member of VDI Fachausschuss Assembly Test, VDI, Frankfurt

K. Pape:
Member of BVS, Bonn

K. Pape:
Member of FED

M. H. Poech:
Member of „Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik"

M. H. Poech:
Member of „Voids"

W. Reinert:
Member of Arbeitskreis A2.6, „Wafernbonden", DVS

W. Reinert:
Speaker of working group „Wafer level packaging" in ZVEI

W. Reinert:
Member of Arbeitskreis A 2.4 Drahtbondtechnik, DVS

W. Reinert:
Member of DVS Fachausschuss Mikroverbindungstechnik

W. Reinert:
Member of ZVEI work group MEMS packaging

W. Reinert:
Member of technical committee of Electronics Packaging Technology Conference (EPTC)-Singapore

W. Reinert:
Member of technical committee of conference Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP)

M. Reiter:
Member of Gf Korr „Arbeitskreis Korrosionsschutz in der Elektronik"

M. Reiter:
Member of „Arbeitskreis Lotpasten"

M. Reiter:
Member of „Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik"

H. Schimanski:
Member of VDE/VDI Arbeitskreis „Prüftechniken in der Elektronikproduktion"

G. Zwicker:
Head of Fachgruppe Planarisierung / Fachausschuss Verfahren / Fachbereich Halbleitertechnologie und –fertigung der GMM des VDE/VDI

G. Zwicker:
Member of International Executive Committee of International Conference on Planarization/ CMP Technology (ICPT)

G. Zwicker:
CMP Symposium Organizer, Material Research Society (MRS), 2007 Spring Meeting, April 10 – April 12, 2007, San Francisco, USA

Cooperation with Institutes and Universities

Centro National de Micro-electronica, Barcelona, Spain

Robert-Koch-Institut, Berlin

Slovac Academy of Sciences, Bratislava, Slovakia

Intl. Centre of Biodynamics, Bukarest, Rumania

Cambridge University, Great Britain

University of Cardiff, Great Britain

University of Coimbra, Coimbra, Portugal

Technische Universität Dresden, Institut für Halbleiter- und Mikrosystemtechnik

Technische Universität, Eindhoven, Netherlands

VTT, Espoo, Finland

University of Exeter, Great Britain

Fachhochschule Flensburg

University of Gdansk, Poland

Ernst-Moritz-Arndt-Universität (EMAU), Greifswald

CEA Leti, Grenoble, France

Hochschule für Angewandte Wissenschaften, Hamburg

Technion, Haifa, Israel

Fachhochschule Westküste, Heide

Technische Universität, Ilmenau

Christian-Albrechts-Universität, Technische Fakultät, Kiel

Fachhochschule Kiel

École Polytechnique Fédérale de Lausanne, Switzerland

IMEC, Leuven, Belgium

Lund University of Technology, Lund, Sweden

Monash University, Melbourne, Australia

ITIA-CNR, Milano, Italy

Wehrwissenschaftliches Institut, Munster

DLR, München

CSEM, Neuchâtel, Switzerland

Sintef ICT, Oslo, Norway

Universität Oulu, Finland

École Polytechnique, Paris, France

University of Pennsylvania, Philadelphia, USA

University of Perugia, Italy

Drexel-University, Philadelphia, USA

University of Pisa, Italy

Royal Institute of Technology (KTH), Stockholm, Sweden

Swedish Defence Research Agency, Stockholm, Sweden

IMS Chips, Stuttgart

VTT, Technical Research Center of Finland, Tampere, Finland

LAAS-CNRS, Toulouse, France

Universität Ulm

Uppsala University, Uppsala, Sweden

Plant Research International, Wageningen, Netherlands

Fachhochschule Vorarlberg, Austria

Vienna Technical University, Wien, Austria

University Wrotzlav, Poland

Fachhochschule Wedel

Distinctions

Bianca Piening
Distiction of being best apprentice as an office clerk at IHK Kiel for which she was awarded by Fraunhofer board member Dr. Dirk-Meints Polter, München, November 2007

Markus Richter
Distiction of being best apprentice as a Mikrotechnologe / focus Microsystems Technology at IHK Kiel for which he was awarded by Fraunhofer board member Dr. Dirk-Meints Polter, München, November 2007

Trade Fairs and Exhibitions

Hannover Messe 2007
April 16 – April 20, 2007, Hannover

SMT Hybrid Packaging 2007
System Integration in Micro Electronics, Exhibition and Conference, April 24 – April 26, 2007, Nürnberg

Laser 2007 World of Photonics
18. International Trade Fair and International Congress, June 18 – June 21, 2007, München

Biotechnica 2007
15. International Trade Fair, Partnering and Conference for Biotechnology, October 9 – October 11, 2007, Hannover

Productronica 2007
17. International Trade Fair for Electronics Production, November 13 – November 16, 2007, München

Miscellaneous Events

Aspekte moderner Siliziumtechnologie
Public lectures.
Monthly presentations, ISIT, Itzehoe

Produktgestaltung: Aktuelles Design for Excellence
Seminar: February 14 and December 5, 2007, ISIT, Itzehoe

Baugruppenfertigung mit Schwerpunkt im Lötprozess
Seminar: February 15 and December 6, 2007, ISIT, Itzehoe

ISIT Presentation for an Institutional Delegation from Biscay, Innovative Incubators
February 27, 2007, ISIT, Itzehoe

Der bleifreie Lötprozess in der Elektronikfertigung
Seminar: February 20 – February 23 and October 9 – October 12, 2007, ISIT, Itzehoe

ISIT Presentation within the Framework of Norderstedt Live BIZ-Club
March 22, 2007, ISIT, Itzehoe

Manuell bleifrei Löten – praxisorientierte Schulung
Seminar: March 20 – March 22 and November 6 – November 8, 2007, ISIT, Itzehoe

SMT-Rework Praktikum – praxisorientierte Schulung – bleifrei
Seminar: March 20 – March 22 and November 6 – November 8, 2007, ISIT, Itzehoe

ISIT Presentation within the Framework of Cooperation Eastern Norway County Network / Schleswig-Holstein, Study Trip to Schleswig-Holstein
April 20, 2007, ISIT, Itzehoe

18. CMP Users Meeting
April 20, 2007, Fraunhofer IMS, Duisburg

Lötprozess II – praxisorientierte Schulung zum „LEADFREE Specialist" an der ISIT-LEADFREE Trainingline
Seminar: May 7 – May 11 and November 26 – November 30, 2007, ISIT, Itzehoe

The RoHS Compliance and its Demands on SMEs – Solutions and Offers of the European Project LEADOUT
June 5, 2007, Itzehoe

Seminar: RoHS Transformation Experiences
June 6, 2007, ISIT, Itzehoe

ISIT Presentation within the Framework of „2. Nacht des Wissens Hamburg"
June 9, 2007, Desy, Hamburg Bahrenfeld

ICPT International Conference on Planarization/CMP Technology (Fraunhofer ISIT, VDE/VDI-Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik)
October 25 – October 27, 2007, Hilton Hotel, Dresden

ISIT Presentation within the Framework of Science Summer School Itzehoe,
October 29, 2007, ISIT, Itzehoe

„JUKI meets friends",
October 31, 2007, ISIT, Itzehoe

ISIT Presentation in the Framework of Fraunhofer Symposium „Innovation Inside",
November 23, 2007, Meilenwerk Berlin

2. Fraunhofer Symposium Micro Energy Technology,
November 27, 2007, Freiburg

Journal Papers, Publications and Contributions to Conferences

T. Ahrens:
Zuverlässigkeitsrisiken Whisker. RoHS-Handbuch für Hersteller und Zulieferer; Praktische Umsetzungshilfen, alternative Materialien und innovative Verfahren, (Editor W. Schruttke, H. Andreae), Kapitel 8.5.1, Forum Verlag Herkert, Merching, update summer 2007

T. Ahrens, O. Lawin, H.-J. Quenzer:
Ein gläsernes Prüfmuster für AOI in der Fertigung elektronischer Baugruppen. Jahrbuch Mikroverbindungstechnik 2007/2008; p. 161 – p. 169, Verlag für Schweißen und verwandte Verfahren, DVS-Verlag, Düsseldorf, 2007

T. Ahrens, M.H. Poech E. Hoefer, S. Wege, T. Lauer, H. Haritz:
Via-in-Pad, Poren, und Zuverlässigkeit bleifreier CSP-Lötverbindungen. Jahrbuch Mikroverbindungstechnik 2007/2008; p. 223 – p. 259, Verlag für Schweißen und verwandte Verfahren, DVS-Verlag, Düsseldorf, 2007

T. Ahrens, M.H. Poech, E. Hoefer, S. Wege, T. Lauer, H. Haritz:
Via-in-Pad, Poren, und Zuverlässigkeit bleifreier CSP-Lötverbindungen. Schweißen und Schneiden 59, Heft 7-8, p. 420 – p. 425, Verlag für Schweißen und verwandte Verfahren, DVS-Verlag, Düsseldorf, 2007

D. Friedrich, H. Bernt, H. Hanssen, P. Oesterlin, H. Schmidt:
Laser Annealing of Power Devices. Proceedings15. IEEE International Conference on Advanced Thermal Processing of Semiconductors, p. 263, Grand Hotel Baia Verde, Catania, Italy, October 2 – October 5, 2007,

S. Guadagnulo, W. Reinert, D. Kähler:
Improved Lifetime Prediction for Vacuum Encapsulated MEMS Packages Utilizing Getter Technology and Leak Rate Screening. Conference on Wafer Bonding for MEMS Technologies and Wafer Level Integration, Halle, December, 2007

E. J. Gómez, M. E. Hernando, T. Vering, M. Rigla, O. Bott, G. Garcia-Sáez, P. Pretschner, E. Brugués, O. Schnell, C. Patte, J. Bergmann, R. Dudde, A. de Leiva:
The INCA System: a Further Step Towards a Telemedical Artificial Pancreas, TITB-00233-2006, IEEE-TITB, 2007

U. Hofmann, S.-N. Baumann:
Mehr Fahrerinformation durch mikrosystemtechnische Laserprojektion.
Photonik, Issue 6/2007, p. 48 – p. 50

T. Lisec:
Preiswerter mikromechanischer RF-Schalter im hermetisch dichten Gehäuse.
Markt & Technik, Edition 44/2007, p. 26 – p. 27

Y. Liu, B. Elsholz, S.-O. Enfors, M. Gabig-Ciminska:
Confirmative Electric DNA arraybased Test for Food Poisoning Bacillus Cereus. J. Microbiol Methods, 2007, 70, p. 55 – p. 64

N. Marenco, W. Reinert, S. Warnat:
Interconnect Challenges in Highly Integrated MEMS/ASIC Subsystems. Proceedings of the Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS, April 25 – April 27, Stresa, Italy, 2007

N. Marenco, W. Reinert, S. Warnat:
DAVID - a Strategic Research Project for Chip-Scale MEMS / ASIC Co-Integration. Proceedings of the IMAPS European Microelectronics and Packaging Conference & Exhibition, June 17 –June 20, Oulu, Finland, 2007

P. Merz, W. Pilz, F. Senger, K. Reimer, M. Grouchko, T. Pandhumpsoporn, W. Bosch, A. Cofer, S. Lassig:
Impact of Si DRIE on Vibratory MEMS Gyroscope Performance. 14. International Conference on Solid-State Sensors, Actuators and Microsystems, Proceedings of Transducers '07, Lyon, France, Vol. 1, p. 1187 – p. 1190, 2007

M. Oldsen, U. Hofmann, H.-J. Quenzer, B. Wagner:
A Novel Fabrication Technology for Waferlevel Vacuum Packaged Microscanning Mirrors.
9. Electronics Packaging Technology Conference, Singapore, 2007

M. Oldsen, U. Hofmann, H.-J. Quenzer, B. Wagner:
Herstellungsverfahren für vakuumgekapselte resonante Mikrospiegel auf Waferebene.
Mikrosystemtechnik Kongress, Dresden, 2007

M.-H. Poech:
Hochstrom-Leiterplatten und geeignete Verbindungstechnologien. SMT/HYBRID/PACKAGING 2007, Tagungsband, VDE Verlag GmbH Berlin Offenbach, p. 151 – p. 159

M.-H. Poech:
Hochstrom-Leiterplatten und geeignete Verbindungstechnologien. PLUS 7/2007

W. Reinert, N. Marenco:
Mikromechanische Sensoren und ASIC in einem Minigehäuse integriert: Mikrosensorik in XXS-Dimensionen.
EPP, Issue February 2007, p. 44 – p. 45

W. Reinert:
Leckraten-Testverfahren: Vakuumdichte MEMS-Gehäuse.
Elektronik Industrie, Issue 3/2007, p. 62 – p. 64

W. Reinert, N. Marenco:
Micromechanical Sensors and ASIC Integrated in a Single Mini Package: Microsensor with Smallest Dimensions. EPP Europe, Issue 3/4/2007, p. 60 – p. 62

W. Reinert:
Industrial Wafer Ball Attach by Gravity Feeding in Comparison to Competing Technologies.
China SMT Forum, Shanghai, May, 2007

W. Reinert:
Leckraten-Testverfahren für resonant betriebene MEMS-Sensoren.
Automotive, Issue 10/2007, p. 58 – p. 60

W. Reinert, P. Merz, K. Reimer:
AuSi Eutectic Seal Bonding for Hermetic MEMS Nano Liter Packages. Conference on Wafer Bonding for MEMS Technologies and Wafer Level Integration, Halle, December, 2007

H. Schimanski:
Hand- und Reparaturlöten – Prozessumstellung setzt intensive Schulung voraus.
Elektronik Praxis, Marktreport Bleifrei 2007 – Auf dem Weg zu grüner Elektronik, March 2007

R. Schmidt, T. Ahrens:
Oberflächeneffekte von Komponenten zum bleifreien Löten Jahrbuch Mikroverbindungstechnik 2007/2008; p. 233 – p. 232, Verlag für Schweißen und verwandte Verfahren, DVS-Verlag, Düsseldorf, 2007

S. Warnat, M. Hoefer, L. Schaefer, H. Foell, P. Lange:
Low Temperature Silicon Nitride Films Deposited on 3D Topography by Hot Wire Chemical Vapor Deposition (HWCVD). Proceedings of MRS Fall Meeting, November 26 – November 30, Boston, MA, USA, 2007

G. Zwicker:
Fabrication of Microdevices Using CMP In: Microelectronic Applications of Chemical Mechanical Planarization, edited by Yuzhuo Li, Wiley Interscience, 2007
ISBN 978-0-471-71919-9

G. Zwicker (Editor and Conference Chairman):
Proceedings of International Conference on Planarization/CMP Technology, October 25 – October 27, 2007, VDE Verlag, Berlin
ISBN 978-3-8007-3065-0

G. Zwicker (Editor):
Advances and Challenges in Chemical Mechanical Planarization, Material Research Society Symposium Proceedings, Vol. 991 (2007)
ISBN 978-1-55899-951-0

Talks and Poster Presentations

T. Ahrens:
DfX: Designprinzipien, Null-Fehler-Strategie, Bauteil-Verfügbarkeit, Chancen durch Rededesign & bleifrei. Seminar: Produktgestaltung: Design for Excellence aktuell, Fraunhofer ISIT, Itzehoe, February 14 and December 5, 2007

T. Ahrens:
Fertigungsgerechtes Baugruppen-Design: Standards für Padlayout, Lotpastendruck, Bestückung, Lötwärmebedarf, bleifrei. Seminar: Design for Excellence aktuell, Fraunhofer ISIT, Itzehoe, February 14 and December 5, 2007

T. Ahrens:
Verantwortung im Design, Einbau der Zuverlässigkeit: Betriebsbelastung, Materialkombination, Anforderungen an Bauteile und Leiterplatten, Entwärmung. Seminar: Design for Excellence aktuell, Fraunhofer ISIT, Itzehoe, February 14 and December 5, 2007

T. Ahrens:
Lötqualität: Lötmetallurgie, Lötoberflächen, Flussmittel. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, Fraunhofer ISIT, Itzehoe, February 20 – February 23 and October 9 – October 12, 2007

T. Ahrens:
Baugruppen- und Fehlerbewertung: Inspektionskriterien, bleifreie Lötstellen. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, Fraunhofer ISIT, Itzehoe, February 20 – February 23 and October 9 – October 12, 2007

T. Ahrens:
Fallstudien bleifreies Löten: Konstruktion, Prozess und Materialauswahl. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, Fraunhofer ISIT, Itzehoe, February 20 – February 23 and October 9 – October 12, 2007

T. Ahrens:
Bleifrei Reparaturlöten: Lote und Flussmittel, Löttemperatur und Wärmebeständigkeit der Materialien. Seminar: Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten, Fraunhofer ISIT, Itzehoe, March 20 – March 22 and November 6 – November 8, 2007

T. Ahrens:
Baugruppen- und Fehlerbewertung: Inspektion, Röntgenverfahren, Querschliffe. Seminar: Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten, Fraunhofer ISIT, Itzehoe, March 20 – March 22 and November 6 – November 8, 2007

A. Conte, S. Guadagnuolo, A. Bonucci, W. Reinert, D. Kaehler:
Improved Lifetime Prediction for Vacuum Encapsulated MEMS Packages Utilizing Getter Technology and Leak Rate Screening. Oral presentation at Wafer bonding workshop, December 12, Halle, Germany, 2007

R. Dudde:
Lithographieverfahren für die Fertigung mikroelektronischer System. Probevorlesung Fachhochschule Wesküste, Heide, April 4, 2007

R. Dudde:
Nanotechnologien – Von der Mikro- zur Nanostrukturierung. Inaugural Lecture for a honory professor Fachhochschule Westküste, Heide, December 7, 2007

P. Gulde, G. Neumann, A. Würsig:
Lithiumakkumulatoren für anspruchsvolle Anwendungen. 14. Design & Elektronik Entwicklerforum, München, March 13, 2007

P. Gulde, G. Neumann, A. Würsig:
Moderne Lithium-Akkumulatoren als leistungsfähige Speicher elektrischer Energie. Institutsseminar Fachbereiche Elektrotechnik, Fachhochschule Kiel, Kiel, December 5, 2007

H. Hanssen:
Nanolöcher und elektrische Anschlüsse für vertikale Caarbon Nanotube Transistoren. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, December 5, 2007

R. Hintsche:
Elektrische Biochip-Technologie – Eine analytische Plattform für Forschung und Praxis. Universität Hamburg, Department Chemie, July 6, 2007

R. Hintsche:
Electrical Biochips – Function and Applications of an Universal Transducer System. Workshop: Molecular Interactions, FU-Berlin, September 5 – September 7, 2007

R.Hintsche:
Portable Analysestysteme mit nanoskaligen elektrischen Biochips für Haptene, Proteine und DNA. 3. BMBF-Symposium Nanobiotechnologie, Messe Hannover, October 9 – October 10, 2007

J. Janes:
Optical Control of RF-Switch Dynamics on Wafer Level. Partest, Itzehoe, April 12, 2007

J. Janes:
RF-Switches. RF-Platform, Barcelona, June 25, 2007

J. Janes:
Control of RF Switch Dynamics. RF-Platform, Barcelona, June 26, 2007

J. Janes:
MEMS Development & Function Control. Süss Microtec, Sacka, July 30, 2007

J. Janes:
RF-Switches & Varicaps. RF-Platform, Paris, October 22, 2007

J. Janes:
Gyro Function Control by Eigen Spectra Analysis. Polytec, Karlsruhe, October 10, 2007

N. Marenco:
Poster presentation of the DAVID project. March 27 – March 28, Smart Systems Integration, Paris, France, 2007

N. Marenco:
Smarte Bewegungssensorik auf vier mal vier Millimetern: Strategische Technologieentwicklung im europäischen Rahmen. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, October 10, 2007

G. Neumann:
Sicherheitsproblematik in Lithium-Hochleistungs-Akkumulatoren. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, April 4, 2007

M. Oldsen:
Vakuumverkapselung von Mikroscannerspiegeln auf Waferebene. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, September 5, 2007

M.-H. Poech:
Das Reflow-Lötprofil: Temperaturverteilung in der Baugruppe. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Bau-gruppen, Fraunhofer ISIT, Itzehoe, February 20 – February 23 and October 9 – October 12, 2007

M.-H. Poech:
Zuverlässigkeit von Lötstellen: Schadensmechanismen, beschleunigte Tests. Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, Fraunhofer ISIT, Itzehoe, February 20 – February 23 and October 9 – October 12, 2007

M.-H. Poech:
Thermisches Management elektronischer Systeme – Teil 2: Bauelemente-Level Auswahl und Beschreibung von Aufbauvarianten, Bauelemente. Haus der Technik, Essen, February 27 – February 28, 2007

M.-H. Poech:
Temperaturprofile für das Reflowlöten. Rehm Technologietag, Blaubeuren, March 8 – March 9, 2007

M.-H. Poech:
Hochstrom-Leiterplatten und geeignete Verbindungstechnologien. SMT 07, Kongress, Nürnberg, April 25, 2007

M.-H. Poech:
Volumeneffekte und technische Zuverlässigkeit bleifreier Lötstellen. 29. Treffen Arbeitskreis „Zuverlässige bleifreie Systeme“, Nürnberg, April 23, 2007

M.-H. Poech:
Qualität und Zuverlässigkeit von porenhaltigen Lötverbindungen an CSPs und anderen Aufbauten. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, June 6, 2007

M.-H. Poech:
Matching Soldering Method and Thermal Design.
ECPE Seminar and Training "LEADFREE Soldering for Power Electronics Manufacturing", ISIT, Itzehoe, June 20 – June 21, 2007

M.-H. Poech:
Solder Joint Reliability.
ECPE Seminar and Training "LEADFREE Soldering for Power Electronics Manufacturing", ISIT Itzehoe, June 20 – June 21, 2007

M.-H. Poech:
High Current PCBs and Suitable Connection Techniques. ECPE Seminar "Passive Components in Power Electronics", Nürnberg, November 22 – November 23, 2007

W. Reinert:
Flip Chip Kontaktierungstechniken: Löten, Kleben und Schweißen.
Technologietag Fa. Würth Elektronik, October, 2007

H. Schimanski:
Qualitätsfaktor Leiterplatte: Prüfmethoden, -standards, Ausfallbeispiele.
Seminar: Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen, Fraunhofer ISIT, Itzehoe, February 20 – February 23 and October 9 – October 12, 2007

H. Schimanski:
Advanced Rework-/ Repair-Technologien hochkomplexer elektronischer Bauten.
15. FED-Konferenz, Bremen, September 13 – September 15, 2007

H. Schimanski
Prozessqualifizierung für schonendes Löten.
Finetech User-Meeting, Berlin, September 27, 2007

S. Warnat:
Post-CMOS kompatible Stromdurchführungen in Halbleitersubstraten.
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, May 2, 2007

Doctoral Theses

B. Elsholz:
Elektrische Mikroarrays für molekulardiagnostische Nachweisverfahren.
Universität Greifswald, December 2007

H. Jacobsen:
Integration von piezoelektrischen Dünnschichten in einen MEMS kompatiblen Prozessablauf auf Waferebene.
Christian-Albrechts-Universität zu Kiel, June 2007

W. Reinert:
Neon Ultra-Feinlecktest zur Vorhersage der Vakuumerhaltung resonanter Mikrosensoren.
Christian-Albrechts-Universität zu Kiel, September 2007

O. Schwarzelbach:
Entwicklung eines mikromechanischen Drehratensensorsystems mit nichtlinearem Anregungskonzept auf der Basis des am ISIT entwickelten PSM-X2-Prozesses.
Christian-Albrechts-Universität zu Kiel, July 24, 2007

Diploma Theses

M. Blehm:
Entwicklung und Konstruktion einer Chipwechselvorrichtung zur automatischen sequentiellen Durchführung mehrerer Messabläufe in einem biotechnischen Analysegerät.
Fachhochschule Flensburg, February, 2007

O. Graak:
Verfahren zur Bewertung von Fehlerbildern mit Methoden der digitalen Bildverarbeitung.
Fachhochschule Flensburg, February, 2007

A. Lemke:
Charakterisierung der Struktur der Morphologie von ZnO Nanorods mit Hilfe der Transmissionselektronenmikroskopie.
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C. Mai:
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A. Schmidt:
Evaluierung und Optimierung von elektrischen Teststrukturen zur Prozesskontrolle von MEMS-Prozessen.
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B. Steible:
Entwicklung und Optimierung von Kupfer-CMP-Prozessen für die Herstellung von RF-MEMS-Bauelementen.
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V. Stenchly:
Ermittlung der Wechsellastfestigkeit von dicken Polysiliziumschichten an oberflächenmikromechanischen Strukturen.
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E. Weit:
Entwicklung einer flexiblen Auswerteelektronik zur Vermesssung von µ-mechanischen Magnetfeldsensoren und Messungen.
Fachhochschule Westküste, Heide, November, 2007

M. Wennholz:
Entwicklung und Optimierung von biologischen Sensoren, so genannten Biochips, zum Nachweis von Proteinen.
Fachhochschule Flensburg, February, 2007

Overview of Projects

- Stand-Off Development for RF High Precision Capacitors
- Development and fabrication of RF High Precision Capacitors
- Support for Build Up a 0,8 µm CMOS Technology
- Support for Build Up a 0,35 µm CMOS Technology
- Development of a Lead Free Sn-Ag Galvanic for WLCSP
- Feedthrough and Wrap Around for Power devices
- Optimierung von AMR Winkelsensoren
- Entwicklung von Cu-Pillars auf Basis dicker Lacke
- Durchkontaktierung von Power Deviecesmittels W-CVD
- Super Junction PowerMOS
- Ultrathin Trench IGBTs on sub-100 µm Si-Substrates
- Carbon Nanotube Devices for Integrated Circuit Engineering
- BCB evaluation for PowerMOS devices
- Untersuchung von Ceroxid-Dispersionen für CMP
- Untersuchung der Polier-eigenschaften verschiedener Slurries für Cu-CMP
- Entwicklung von poly-Si CMP Prozessen für die MEMS Herstellung
- Untersuchung an mikromecha-nischen Drehraten-Sensoren
- Entwicklung von kapazitiven HF-Schaltern
- Entwicklung von piezo-elektrischen Schichten für Si-Mikroaktuatoren
- Ultraschallanalyse flüssiger Mehrphasengemische
- Herstellung mikrooptischer Linsenarrays aus Glas
- AMICOM: Advanced MEMS for RF and Millimeter Wave Communications, Network of Excellence
- RF-MEMS Packaging
- Drehratensensoren für Raumfahrtanwendungen
- Piezoelektrischer Messkopf für die Ultraschallanalytik
- Entwicklung von Messstrategien zur Evaluierung von Parametern für MEMS Design
- Mikroscann-Systeme für Display Anwendungen
- Mikrotechnische Fabrikation von Laserresonator Spiegeln
- Herstellung mikrotechnischer analogen Ablenkeinheiten
- Charged Particle Nanotech, CHARPAN
- Radical Innovation Maskless Nanolithography, RIMANA
- Mikrosystemtechnische Laserprojektion zur infor-matorischen Fahrerassistenz, MICLAS
- Study on Silicon MEMS Force Sensors, SMErobot
- Entwicklung eines Motor-Ansteuer-ASICs
- Development of an ASIC for the control of BLDC-motors
- Probebased terabit memory. PROTEM
- Generic Manufacturing and Design Technology Platforms Based on Novel RF Technologies, RF-PLATFORM
- Customer Support and Design Centre for Physical Measure-ment Systems, EUROPRACTICE CCMeSys
- Microactuator Competence Centre, EUROPRACTICE CCMicro
- Electrical Bio Sensor Arrays for Analyses of Harmful Micro Organisms and Microbial Toxins, eBiosense
- Genotype-Specific Hepatitis C Diagnostic Chip, HCV
- Entwicklung biochemischer Erkennungssysteme für portable elektrische Detektionssysteme von Biowaffen-Toxinen
- Elektrischer DBD-ISIT-eBS-Array-Immundetektor: Beratung, Bereitstellung und Spotten von Mikrochips für den Toxin-nachweis, Service
- Analysesystem für die marker-gestützte intraoperative Tumor-diagnostik
- USDEP, Ultrasensitive Detection of Emerging Pathogens
- ivD-MAVO, in vitro Diagnostik Plattform
- Chipkartenbestückung mit Grautonblenden
- Stressoptimierte Montage und Gehäusetechnik für mikro-mechanisch hergestellte Silizium-Drehratensensoren
- Glassfritt Vacuum Wafer Bonding
- Glaslotbonden mit strukturierten Capwafern und Musterwafern
- Automotives Mikrokamera-system für Fahrzeugumfeld-erfassung, µ-CAM
- Downscaled Assembly of Vertically Interconnected Devices, DAVID
- Pan-Mobile Erfassung mit optimierten Smart-Labels zur Effizienzsteigerung von Logistikprozessen, PESEL
- Wafer Level Packaging
- Wafer Level Balling for 100 µm up to 500 µm Spheares
- Customer specified test wafers
- Neon ultra fine leak test for resonant micro sensors
- Solder flip chip on flex
- ACF flip chip assembly on semirigid substrate
- Flip chip embedding study and demonstration
- Volumeneffekte und technische Zuverlässigkeit von bleifreien Lötstellen
- Qualitätsbewertung an bleifreien Baugruppen
- Demonstration and Training Lead-Free Soldering for European Industrie, LIFE
- Untersuchung zu den thermi-schen und prozesstechnischen Eigenschaften von Flussmitteln für bleifreie Lötlegierungen auf hochzuverlässigen Baugruppen
- Systemaufbau eines Energie-speichers für die Plug-In Hybridfahrzeuge
- Materialscreening von Elektrodenmaterialien für Lithiumakkumulatoren zum Einsatz in Hybrid- und Elektrofahrzeugen
- Studie: Lithiumakkumulatoren zur Zwischenspeicherung von Solarstrom
- Studie: Ersatz des Bleiakkumu-lators als Starterbatterie durch Lithiumakkumulatoren

Patents

J. Albers, H. Bernt, R. Bredehorst, R. Hintsche, R. Seitz
Sensor Arrangement With Electrically Controllable Arrays
US 7 208 077 B1

J. Albers, H. Bernt, R. Bredehorst, R. Hintsche, R. Seitz
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EP 1 200 817 B1

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Dotierung von Halbleiterbauelementen insbesondere für die Solartechnik
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P. Birke, G. Neumann
Pasty materials with nanocrystalline materials for electrochemical components and layers and electrochemical components produced with said materials
KR 0777504

P. Birke, G. Neumann
Pasty materials comprising inorganic, fluid conductors and layers produced therefrom, and electrochemical components made from these layers
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P. Birke, F. Salam-Birke
Self-supporting layer and a method for producing the same
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In elektrochemischen Bauelementen verwendbare pastäse Masse, damit gebildete Schichten, Folien, Schichtverbünde und wiederaufladbare elektrochemische Zellen sowie Verfahren zur Herstellung der Schichten, Folien und Schichtverbünde
DE 199 52 335 B4

P. Birke, G. Neumann
Paste-like mass for the preparation of solid body electrolyte layers
IN 207720

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Paste-like masses for electrochemical elements and layers and electrochemical elements produced therefrom
IN 203330

P. Birke, G. Neumann
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Films for electrochemical components and method for producing the same
ZL 00815133.4

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Method of examining and/or modifying surface structures of a sample.
JP 392 1347

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DE 10 2005 053 722 B4

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Beam-shaping element for optical radiation and a method for producing said element
US 7,286, 294 B2

H. J. Quenzer, B. Wagner
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EP 1 269 506 B1

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Elektrolyte für elektrochemische Bauelemente
DE 102007031477.0-45

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